

Curriculum Vitae

Mail Address:

5030 Centre Ave #359
Pittsburgh, PA, 15213

Phone

Office : 1 412 268 9499
Cellular: 1 858 232 7552

Webpage:

<http://www.ece.cmu.edu/~pdalbert>

Email

: paolo.dalberto@gmail.edu

Education

- Post-doctorate fellowship Carnegie-Mellon University Dept. Electric and Computer Science, 2005-Present.
- Ph.D. in Computer Science, University of California at Irvine, 2005
 - Dissertation: “**The X- Legion: a compiler-approach to exploit locality and portability of divide-and-conquer algorithms**”
(Advisor Prof. A. Nicolau)
- Dottorato di ricerca, Computer Science, University of Bologna, Italy, 2000
 - Thesis title: “**Performance evaluation of Data exploitation**”
(Advisor Prof. G. File’)
- First modulo of Master in Software Engineering, Tecnopadova and S.E.R.C. Padua, Italy.
- B.S. In Electrical and Computer Engineering, University of Padua, Italy.
 - Thesis title: “**Space Complexity of DAG Computations in Memory Hierarchies**” (Advisor Prof. G. Bilardi)

Post-Doc

Summary: I have investigated and developed Software/Hardware partitioning techniques for DSP applications using the SPIRAL framework in embedded systems/processors such as VirtexII/XScale.

Ph.D Dissertation

Summary: I have investigated compiler techniques for the analysis of data locality in Divide-and-Conquer algorithms – especially, Linear Algebra applications – both recursive and non-recursive and the techniques utilization to drive novel memory hierarchy adaptations (statically and at run time).

Awards and Sponsors

- (2005-present) DARPA through the Department of Interior grant NBCH1050009
- (2005) Dissertation Fellowship University of California Irvine
- Scholarship award made by Alpha Association of Phi Beta Kappa Alumni in Southern California (2003)
- (2000-2002) Research sponsored in part by DARPA/ITO under contract DABT63-98-C-0045.
- Research sponsored in part by NSF under contract ACI-0204028.

Publications

In Journals

- P.D'Alberto, A.Nicolau, A. Veidenbaum and R.Gupta: **"Line Size Adaptivity Analysis of Parameterized Loop Nests for Direct Mapped Data Cache"**. Published in Transactions on Computers, IEEE Society, Feb 2005.
- P.D'Alberto and A. Nicolau **"R-Kleene: A High-Performance Divide-and-Conquer Algorithm for the All-Pair Shortest Path for Densely Connected Networks"**. Algorithmica (2007)

In Book Chapters

- P.D'Alberto, A.Veidembaum, A.Nicolau and R.Gupta: **"Static Analysis of Parameterized Loop Nests for Energy Efficient Use of Data Caches"**. Workshop on Compilers and Operating Systems for Low Power 2001 (COLP01) - Chapter in a Kluwer book.

In Conferences/Workshops

- P.D'Alberto and A. Nicolau **"Adaptive Strassen's Matrix Multiplication"**, To be presented at the 21th International Conference on Supercomputing
- Paolo D'Alberto, Peter Milder, Aliaksei Sandryhaila, Franz Franchetti, James Hoe, Jeremy Johnson, Jose' Moura, and Markus Pueschel **"Generating FPGA-Accelerated DFT Libraries"**, To be presented at the Field-Programmable Custom Computing Machines IEEE Symposium (FCCM) 2007
- P.D'Alberto, F.Franchetti, and M.Pueschel **"Performance/Energy Optimization of DSP Transforms on the Scale Processor"**. International Conference on High Performance Embedded Architectures & Compilers 2007
- P.D'Alberto, P.Milder, F.Franchetti, J.C.Hoe, M.Pueschel and J.Moura **"Discrete Fourier Transform Compiler for FPGA and CPU/FPGA Partitioned Implementations"** The 10th Workshop High performance Embedded Computing (2006)
- P.D'Alberto and A. Nicolau **"Adaptive Strassen and ATLAS's DGEMM: A Fast Square-Matrix Multiply for Modern High-Performance Systems"**. The 8th International Conference on High Performance Computing in Asia Pacific Region (HPC asia) 2005

- P.D'Alberto and A. Nicolau “**Using Recursion to Boost ATLAS's Performance**” The Sixth International Symposium on High Performance Computing (ISHPC-VI) 2005
- P.D'Alberto and A.Nicolau: “**JuliusC: A Practical Approach for the Analysis of Divide-And-Conquer Algorithms**”. The 17th International Workshop on Languages and Compilers for Parallel Computing, LCPC 2004
- Kejariwal, P.D'Alberto, A.Nicolau and C.D.Polychronopoulos: “**A Geometric Approach for Partitioning N-Dimensional Non-Rectangular Iteration Space**”. LCPC 2004
- P. D'Alberto, A.Nicolau and A.Veidenbaum: “**A Data Cache with Dynamic Mapping**”. LCPC 2003.
- G.Bilardi, P.D'Alberto and A.Nicolau: “**Fractal Matrix Multiplication: a Case Study on Portability of Cache Performance**”. Workshop on Algorithm Engineering WAE 2001
- G.Bilardi, A.Pietracaprina and P.D'Alberto: “**On the space and access complexity of computation DAGs**”. Workshop on Graph-Theoretic Concepts in Computer Science 2000

In Technical Reports

- H.Du, P.D'Alberto, R.Gupta, A.Nicolau and A.Veidenbaum: “**A quantitative evaluation of adaptive memory hierarchy**”. UCI Technical Report (2002)
- P.D'Alberto: “**MIPS R12000 Processor Performance Evaluation by SPEC2000 Benchmarks and Performance Counters**”. UCI Technical Report (2001)
- P.D'Alberto: “**Fractal LU-decomposition with partial pivoting**”. UCI TR (2001)
- P.D'Alberto: “**Performance Evaluation of Data Locality Exploitation**”. (2000 University of Bologna Technical Report – Thesis)

All publications are available in electronic format at
<http://www.ece.cmu.edu/~pdalbert/Reference/reference.html>

Professional Experience

Teaching Experience:

- **Computer Science, University of California at Irvine**
Taught and designed the curriculum and tests
 - **Lecturer**, Fall 2004.
Introduction to computer systems (lower division class)
 - **Lecturer**, Summer 2004.
Compilers and Interpreters (upper division class)
 - **Lecturer**, Fall 2003.
Language Processor Construction (upper division class)
- **Computer Science and Engineering, University of California at San Diego**
Taught and designed curriculum and tests

- **Lecturer**, Summer 2003.
Compiler construction I (upper division class).
- **Computer Science, University of California at Irvine**
Leaded discussions and designed tests
 - **Teacher assistant**, 2002-2004
Compilers and Interpreters (upper division class)
 - **Teacher assistant**, Fall 2003
Language Processor Construction (upper division class)
- **Tecnopadova and S.E.R.C**
 - **Coordinator/Lecturer**, 1997.
First modulo of Master in Software Engineering.

Other Experiences:

- Contributor in the preparation, organization and final presentation of fund proposals to institutions/organizations such as DARPA, NFS, Motorola (3years -100K\$) and NASA (4years - 12M\$).
- *Research Assistant*, Department of Computer Science, UCI, 1998-2004.
- Software-engineer consultant for SEIT Electronics, Valdobbiadene, Treviso, Italy. Jul. 1995 - Mar. 1996: Project: Software design of real-time applications for high frequency soldering machines (a Unix-based simulation environment for micro-controlled high frequency soldering machines).

Professional Memberships and Activities

- SIAM Member since 2006.
- Reviewer for international conferences, workshops (e.g., ICS, LCPC, MICRO, PACT, SCOPE, ICCAD, DATE, DAC, SBCCI) and journals (e.g., the International Journal for Parallel Programming (IJPP), ACM Transaction on Embedded Computing Systems, IEEE Transaction on Very Large Scale of Integration. IEEE Transactions on CAD).

Computer Skills:

- **Languages:** C/C++, Java JDK, perl, LaTeX, HTML, XML, FORTRAN, Prolog
- **Tools:** lex, bison, Microsoft Office, openOffice, matlab, gcc, etc.
- **Operating Systems:** Windows, Unix , Fedora
- **Web-service:** apache server.

