Student ID: _____

CS 151
Final

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **16 pages** including this cover.
2. Write down your Student-Id on the top of each page of this final.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this final are **110 + 20 EXTRA CREDIT.**
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

	PART I	PART II	PART II (Extra Credit)
Total Credit	**50**	**60**	**20**

Student ID: _____

PART I – Short Questions

In this section you need to show your work.

Q1: [Algebraic Manipulation] [5 Points]

Algebraically prove the following:

x'y'z' + xyz' + xyz + xy'z' + x'yz' = z' + xy

Q2: [2's Complement operation] [5 Points]

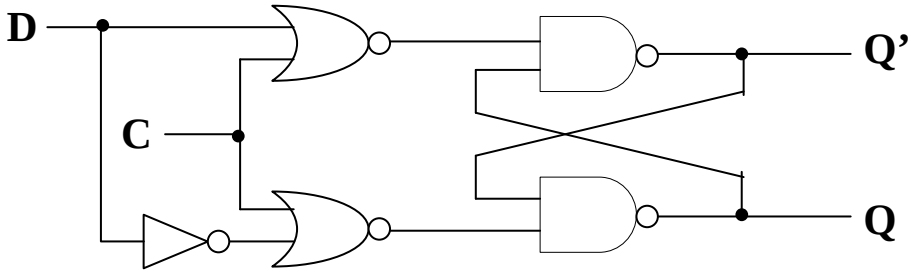
Using two's complement method show the result for the following operation:

101110 – 1110 =

Student ID: _____

Q3: [Latch Analysis] [10 points]

Shown below is a NOR and NAND implementation of gated D-latch:

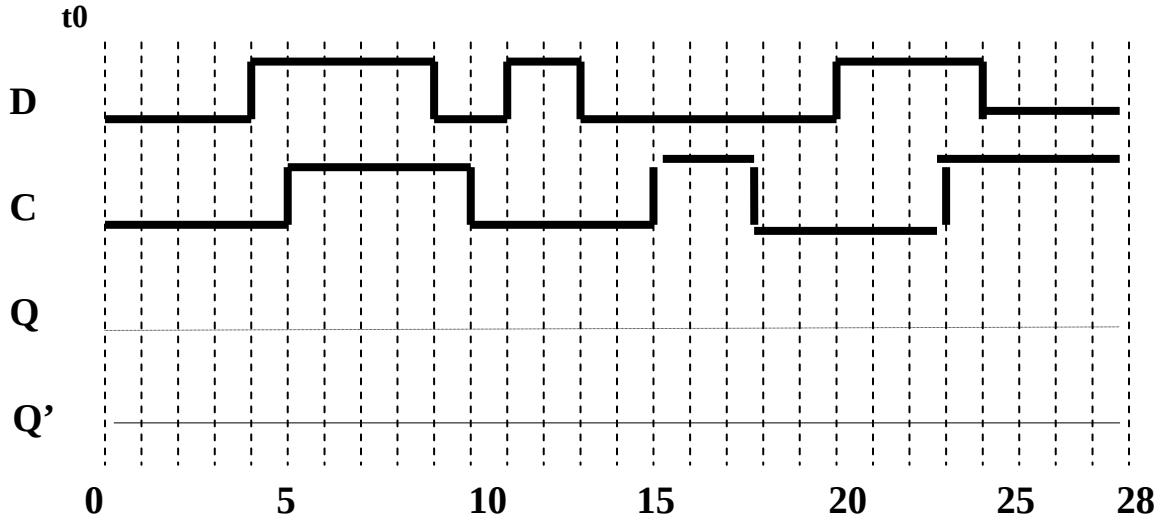


For the following timing diagram of inputs:

- fill in the following table for the value of Q given the inputs C and D, and
- draw the timing diagrams for outputs Q and Q' in the timing diagram

(**Assume that Q=0 at t0 and there is no gate delay**)

C	D		Q
0	0		
0	1		
1	0		
1	1		



Student ID: _____

Q4: [Hierarchical DeMultiplexer Design] [10 points]

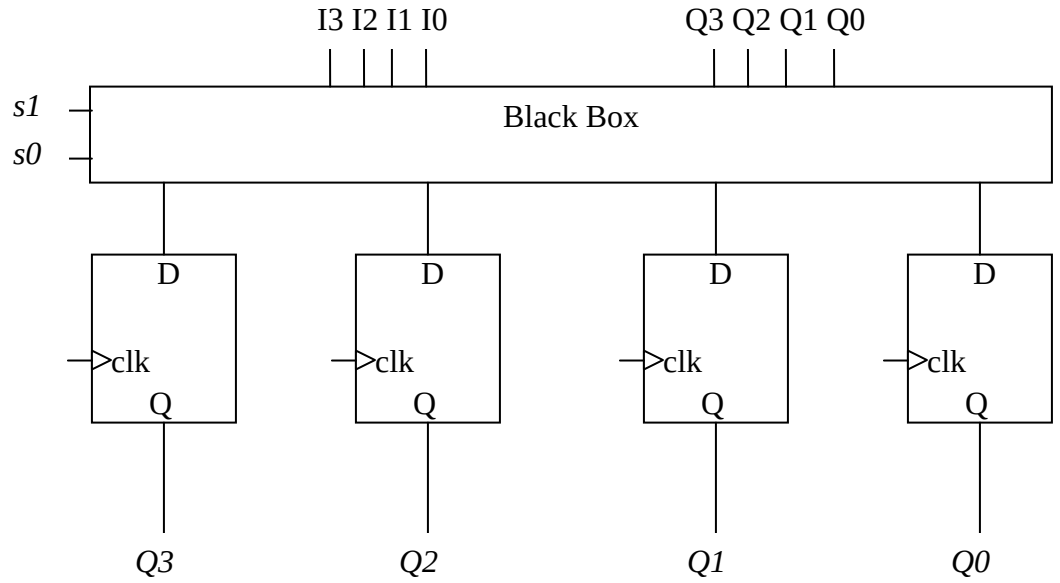
Design a 1-to-16 DeMultiplexer using **ONLY** 1-to-4 DeMultiplexers.

Student ID: _____

Q5: Register Design [10 points]

Design a 4-bit register with 2 control inputs s_1 and s_0, 4 data inputs $I_3..I_0$, and 4 data outputs $Q_3..Q_0$. The function table below shows the configurations for the register.
In this question you have to design the circuit inside the "Black Box".

S1	S0	Action
0	0	Keep the current value
0	1	Load I
1	0	Clear the content of the register
1	1	Rotate left by one bit



<This page is intentionally left blank>

Student ID: _____

Q6: [Karnaugh Map] [10 Points]

In the following K-Map specify the prime implicants and the essential prime implicants and write the reduced function form:

X_1X_0 \ Y_1Y_0	00	01	11	10
00	0	0	X	X
01	1	0	0	X
11	1	1	0	1
10	1	1	0	X

Student ID: _____

PART II – Design Questions

Q1: [Counter-based Design] [20 points]

Using a 4-bit counter and minimum number of the following components design a circuit which outputs the following sequence: 3 -> 6 -> 9 -> 12 -> 25 -> 30 -> 35 -> 40

a) Comparator
b) Shifter
c) Adder
d) Subtractor
e) Multiplexer

HINT: Think about the sequences 3 -> 6 -> 9 -> 12 -> 15 -> 18 -> 21 -> 24 and 5 -> 10 -> 15 -> 20 -> 25 -> 30 -> 35 -> 40 to solve the problem.

<This page is intentionally left blank>

Student ID: _____

Q2: C to RTL design [40 points]

Consider the following C code which you want to eventually implement in hardware:

```
 1. int Search(int image[])
 2. { int nComp=0, val, valOld, x0, y0;
 3.   for (y0=0; y0 < 10; y0++)
 4.   { valOld=0;
 5.     for (x0=0; x0 < 15; x0++)
 6.     { val=image[x0+15*y0];
 7.       lab=image[x0+15*y0];
 8.       if ((val > 0) && (valOld == 0))
 9.       { nComp++;
10.       }
11.       valOld=val;
12.     }
13.   }
14.   return nComp;
15. }
```

Student ID: _____

a.i) Derive the high-level state machine of this code. (Exploit as much concurrency as possible.) **[10 Points]**

a.ii) Allocate data path components for fastest design and bind the operators to the components. **[10 Points]**

b.i) Derive the high-level state machine with the minimal number of resources. (i.e, exploiting resource sharing which results in the “smallest” design.) **[10 Points]**

b.ii) Allocate data path components for this smallest design and bind the operators to the components. (Assume the size of a multiplexer is much smaller than the size of the data path components) **[10 Points]**

Student ID: _____

[Extra Credit]Controller design [20 points]

1. For the high-level state machine and the datapath designed in Q2.b.i and Q2.b.ii design the interface to the system and the interface of controller and the datapath. **[5 Points]**

2. Design the FSM for the controller. **[15 Points]**