Student ID: _____

CS 151
Quiz 7

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

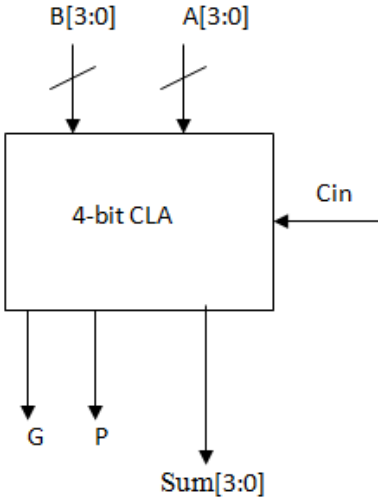
Instructions:

1. Please verify that your paper contains **8 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **60 points.**
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

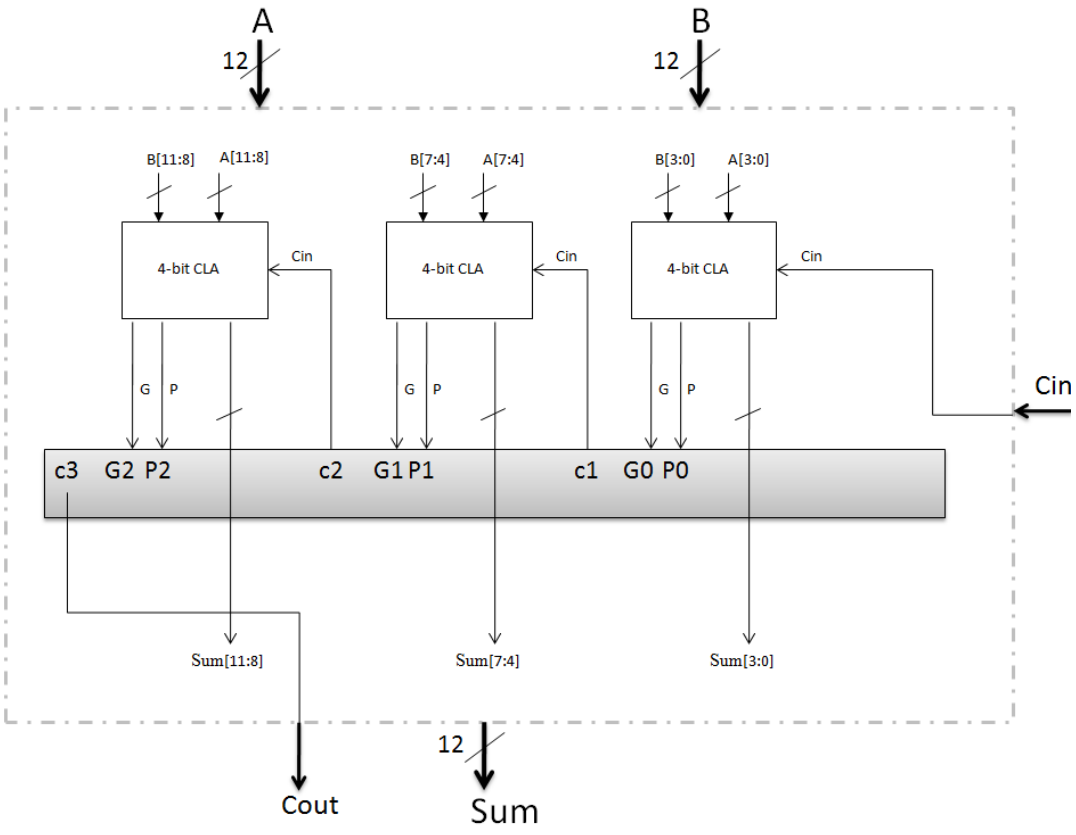
Student ID: _____

Q1 [Carry Look-Ahead adder] [30 points]

In this problem we are going to design a 12-bit hierarchical carry look-ahead (CLA) adder out of 4-bit CLA components (as shown below). **[15 points]**



a) Draw the interface between the 4-bit CLAs and the CLA Logic that should be added to implement the 12-bit adder. Use the black box below. (At this stage you do not need to implement the circuit inside the blocks.) **[15 points]**



Student ID: _____

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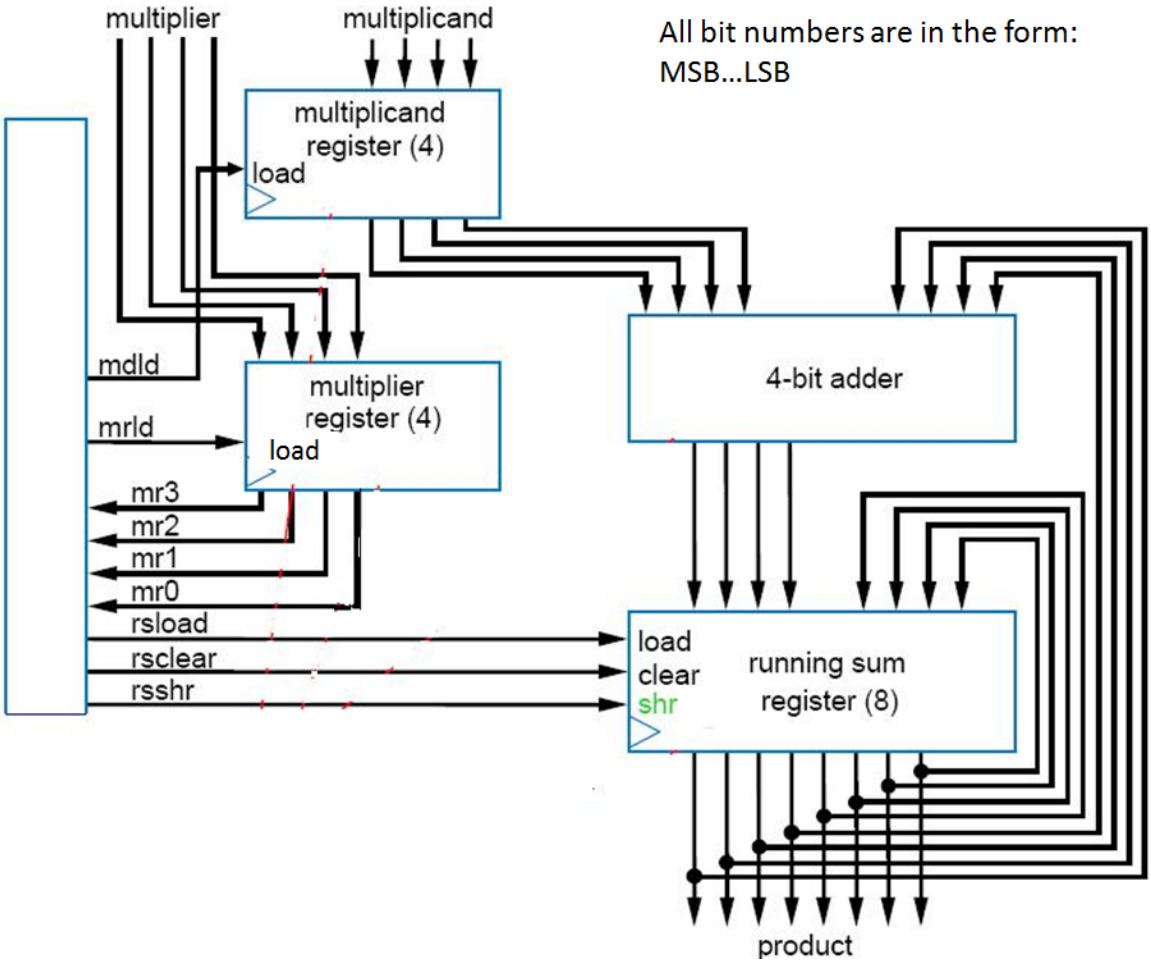
b) Write the equations for the outputs of the CLA Logic block. **[15 points]**

C1 = G0 + P0C0
C2 = G1 + P1C1 = G1 + P1(G0 + P0C0) = G1 + P1G0 + P1P0G0
C3 = G2 + P2C2 = G2 + P2(G1+ P1C1) = G2 + P2(G1 + P1G0 + P1P0G0) = G2 + P2G1 + P2P1G0 + P2P1P0G0

Student ID: _____

Q2 [Add and Shift Multiplier] [15 points]

We want to multiply two 4-bit unsigned binary numbers using add and shift method with a data path shown below. The **multiplicand** is equal to 0101 and the **multiplier** is equal to 0111. The table on the next page shows an algorithmic step-by-step view of the process and the contents of registers Multiplicand, Multiplier and Running Sum. We have filled on the first 5 steps. Complete the table for executing the multiplication until it is done and show content of the registers after each step of adds and shifts.



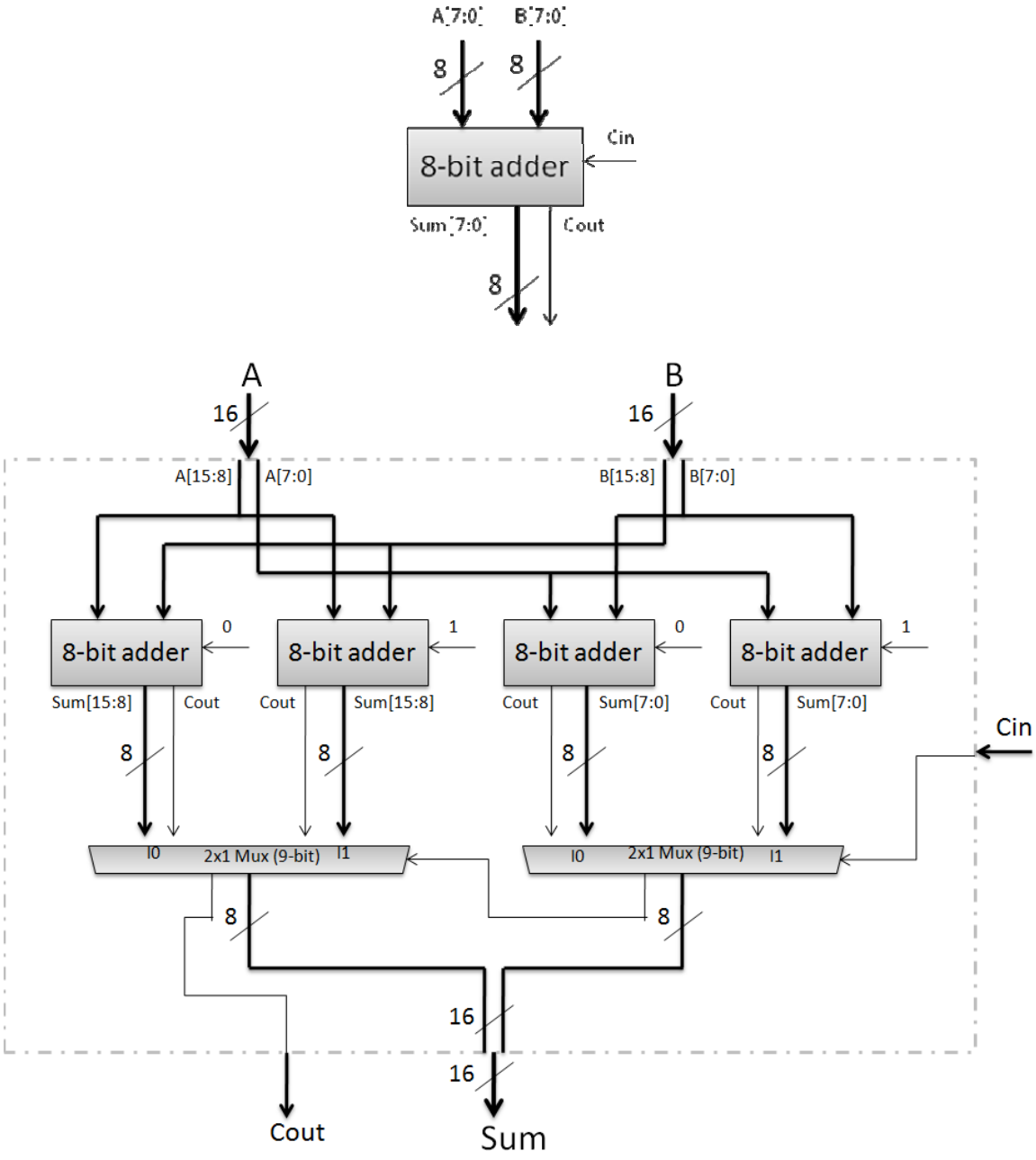
Student ID: _____

Step	Action	Multiplicand reg (md)	Multiplier reg (mr)	Running Sum reg (rs)
1	**Load mr**	**0101**	**0000**	**00000000**
2	**Load md**	**0101**	**0111**	**00000000**
3	**Check mr0**			
4	**Load rs (rs = rs+md)**	**0101**	**0111**	**01010000**
5	**Shift right rs**	**0101**	**0111**	**00101000**
6	**Check mr1**			
7	**Load rs (rs = rs+md)**	**0101**	**0111**	**01111000**
8	**Shift right rs**	**0101**	**0111**	**00111100**
9	**Check mr2**			
10	**Load rs (rs = rs+md)**	**0101**	**0111**	**10001100**
11	**Shift right rs**	**0101**	**0111**	**01000110**
12	**Check mr3**			
13	**Shift right rs**	**0101**	**0111**	**00100011**
Done	**Done**	**0101**	**0111**	**00100011**

Student ID: _____

Q3 [Carry Select Adder] [15 points]

Design a 16-bit carry select adder out of 8-bit adders and multiplexers. Below is the diagram of a 8-bit adder.



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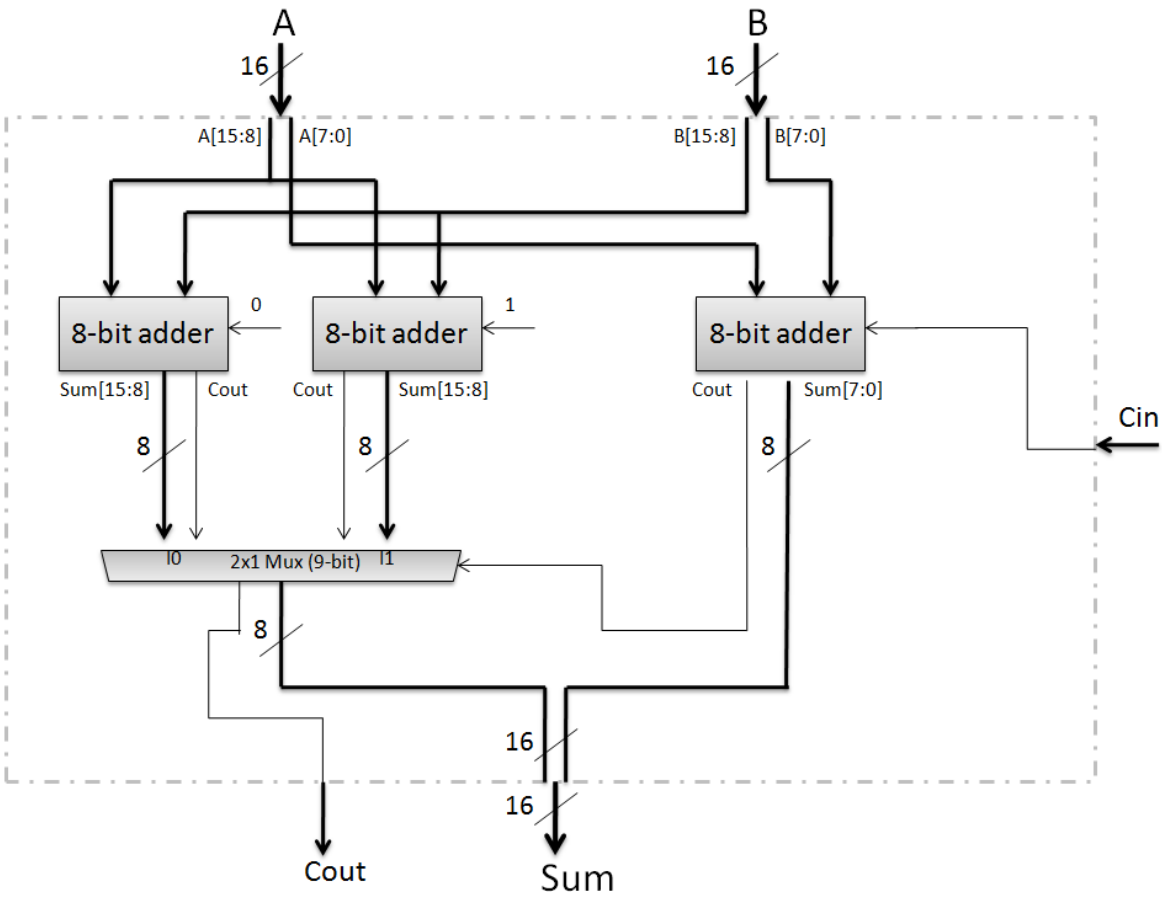

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