

Student ID: _____

CS 151 Final

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

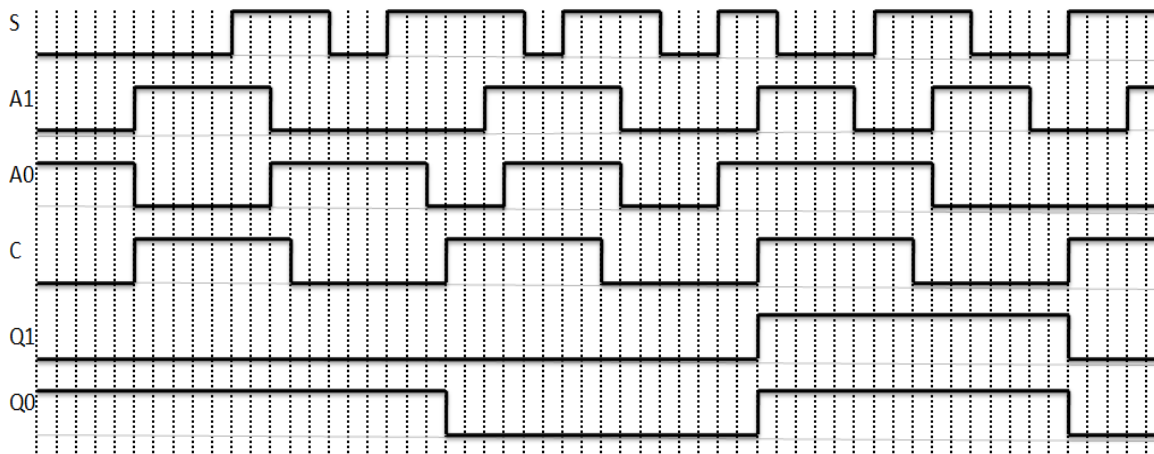
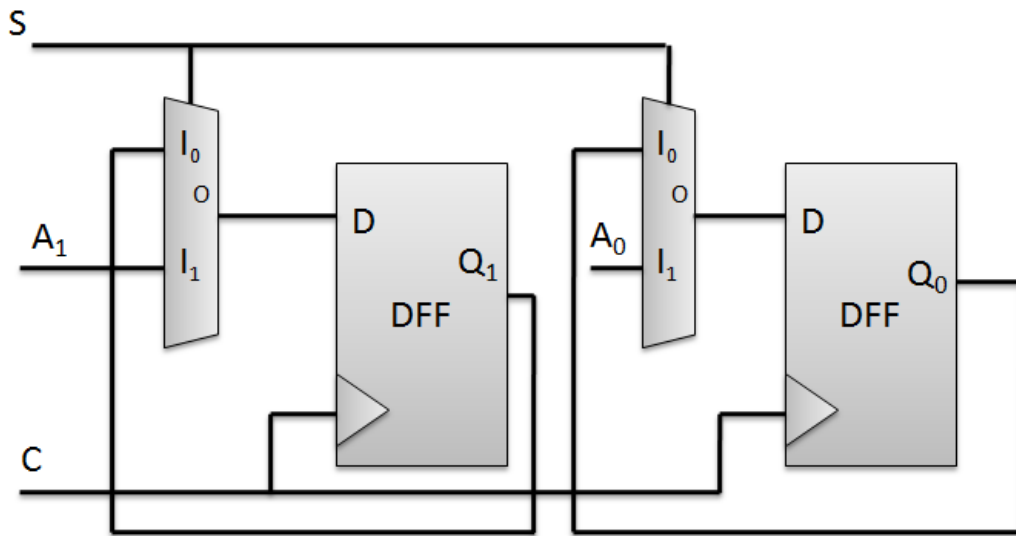
1. Please verify that your paper contains **20 pages** including this cover.
2. Write down your Student-Id on the top of each page of this final.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this final are **115 + 10 EXTRA CREDIT**.
5. To receive credit you must show your work clearly.
6. Calculators are **NOT** allowed.
7. If necessary, state your assumptions clearly.

Total	Q1	Q2	Q3	Q4	Q5	Q6	[Extra Credit]
115+10	10	10	20	15	40	20	10

Q1: [Sequential Circuit Timing Analysis]**[10 Points]**

The circuit below shows a sequential circuit using D Flip Flops, and Multiplexers. Assuming that A_1 , A_0 , and S are the inputs of the circuit, and Q_1 is 0, Q_0 is 1 when time equals 0 (t_0), show the timing diagram for Q_1 and Q_0 .

NOTE: You can assume that gate delay is negligible.

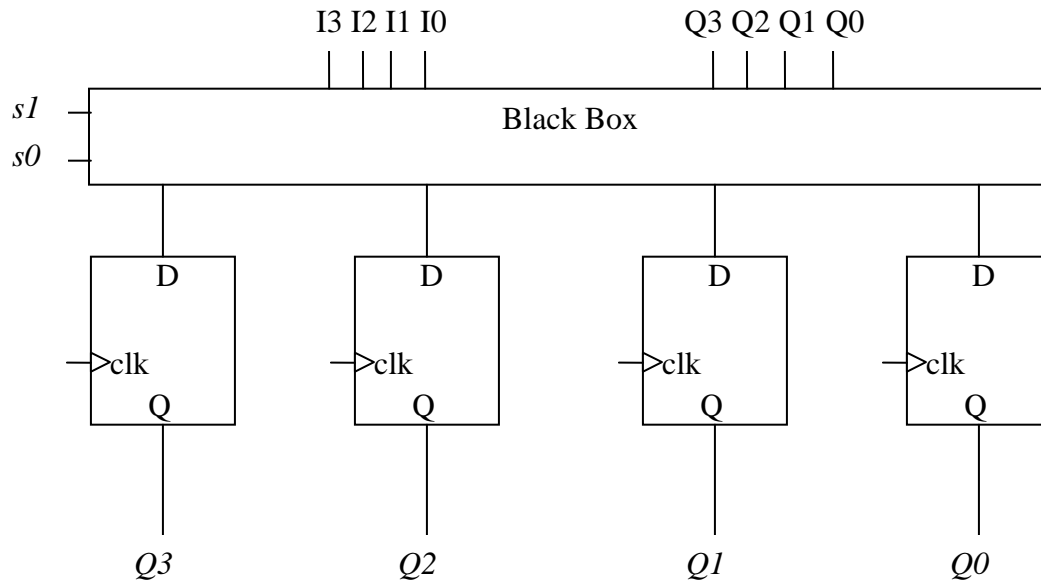


Q2: [Register Design]**[10 points]**

Design a 4-bit register with 2 control inputs s_1 and s_0 , 4 data inputs $I_3..I_0$, and 4 data outputs $Q_3..Q_0$. The function table below shows the configurations for the register.

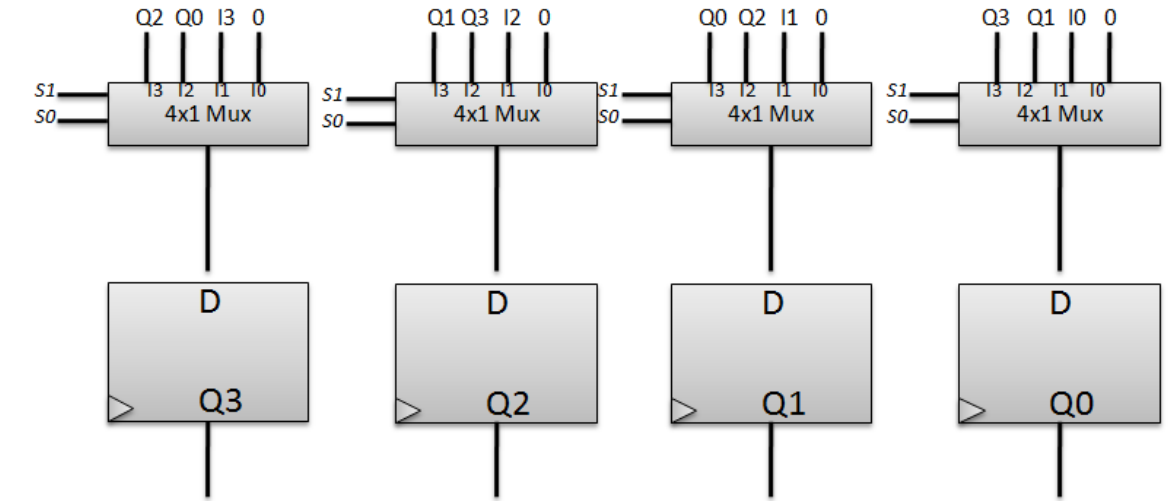
In this question you have to design the circuit inside the “Black Box”.

S1	S0	Action
0	0	Clear the contents of the register
0	1	Load I
1	0	Rotate right by one bit
1	1	Rotate left by one bit



Student ID: _____

<This page is intentionally left blank>



Student ID: _____

Q3: [Counter-based Design] [20 points]

Using **only a 4-bit up** binary counter, you are going to design a circuit that detects odd numbers in a sequence of numbers, its output (denoted by **ODD**) is 1 when the sequence value is an odd number, 0 otherwise. The sequence is defined below in Q3a. You can use any of the following components (**Specify the bit widths, and name all inputs/outputs**):

- 1) Adders
- 2) Shifters
- 3) Comparators
- 4) Multiplexers
- 5) Subtractors

Make sure you answer both parts 3a, and 3b.

3a. Using the 4-bit up binary counter, create a circuit that generates the following sequence [10 points]:

48 → 45 → 42 → 39 → 36 → 33 → 30 → 27 → 24 →
21 → 18 → 15 → 12 → 9 → 6 → 3 → 48 → 45 → 42 ...

Student ID: _____

<This page is intentionally left blank>

4-bit up counter counts from 0000 (0) to 1111 (15), and then it re-starts its counting sequence

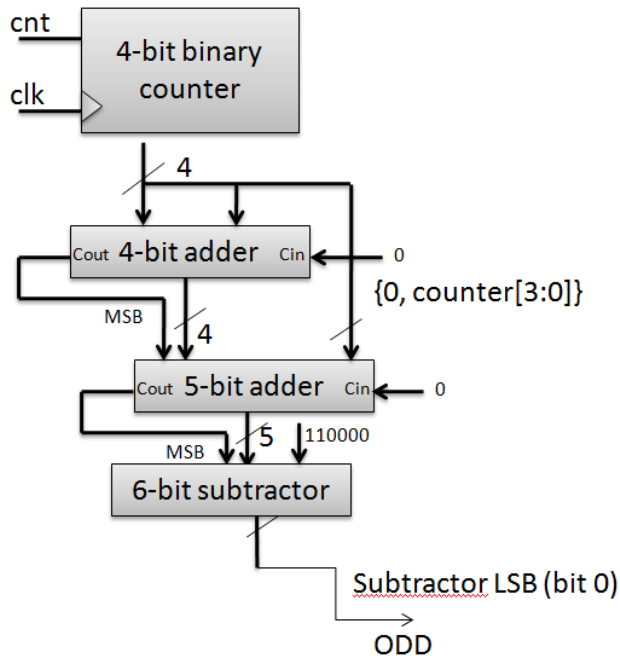
Sequence: $48 \rightarrow 45 \rightarrow 42 \rightarrow 39 \rightarrow 36 \rightarrow 33 \rightarrow 30 \rightarrow 27 \rightarrow 24 \rightarrow$

$21 \rightarrow 18 \rightarrow 15 \rightarrow 12 \rightarrow 9 \rightarrow 6 \rightarrow 3 \rightarrow 48 \rightarrow 45 \rightarrow 42$

$48 = nx + k$, take $x=0$, $48 = n(0) + k \Rightarrow 48 = k$

$48 = nx + 48$, take $x = 1$, $45 = n(1) + 48 \Rightarrow 45 = n + 48$, $n = -3$

So, the equation is given by $48 - 3n$, could be represented as $48 - (2n + n)$



We are looking for odd numbers
so, every odd number represented
In binary has the LSB, or
bit 0 = 1

000001 = 1 = odd
000010 = 2 = even
000011 = 3 = odd
100000 = 32 = even
100001 = 33 = odd
...

So, let's just check the last bit for a 1
If it is not 1, then we know that the
Number is even, and ODD = 0,
Otherwise, ODD=1, so there is a
One to one mapping between the lsb
And whether a number is odd, or even
So, we can use the lsb as our output
signal

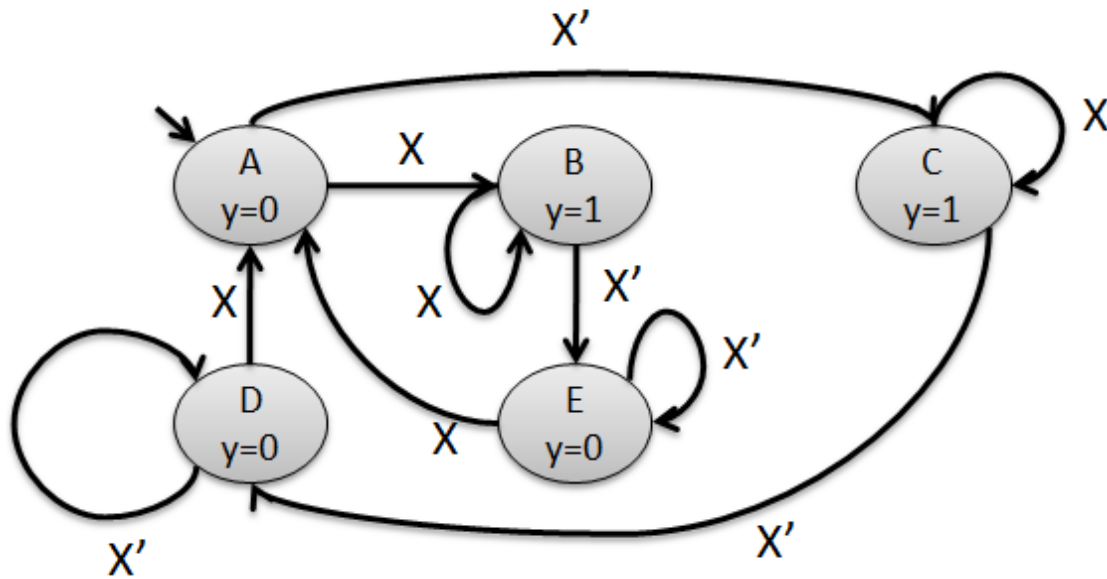
Student ID: _____

3b. Using the circuit designed in part 3a, modify it so that whenever an odd number is encountered in the sequence generated, your circuit outputs a 1 (ODD signal is 1), otherwise, it outputs a 0. [5 points]

Q4: [State minimization]

[15 points]

4a. Reduce the number of states in the following state machine using the implication table method. Which states are the same? [10 points]

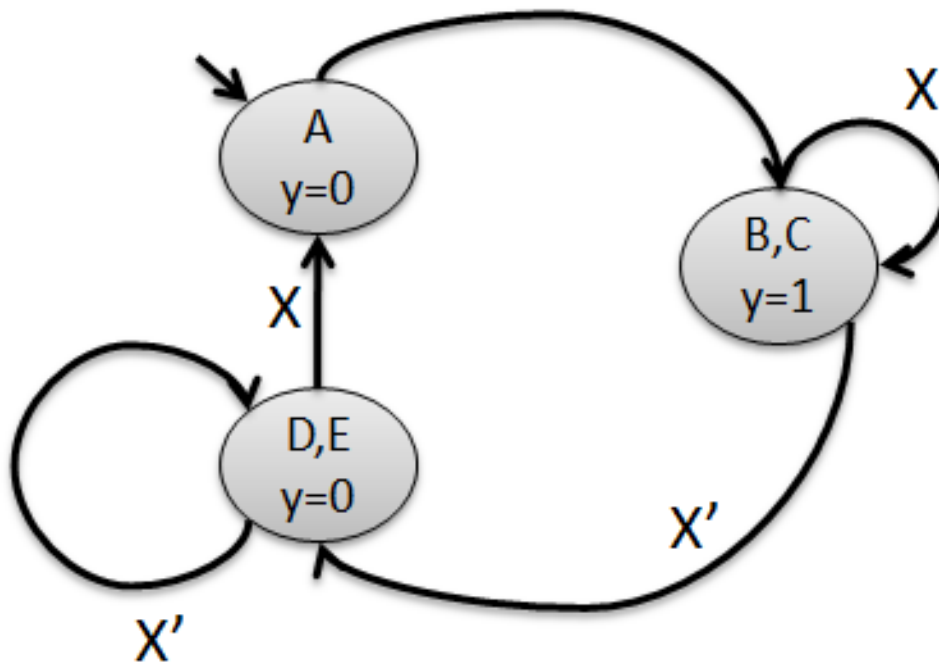


<u>A</u>					
<u>B</u>	X				
<u>C</u>	X	(D,E) (C,B)			
<u>D</u>	(D,C) (A,B)	X	X		
<u>E</u>	(E,C) (A,B)	X	X	(E,D) (A,A)	
	<u>A</u>	<u>B</u>	<u>C</u>	<u>D</u>	<u>E</u>

Student ID: _____

4b. Draw the reduced state machine below. [5 points]

C=B, D=E



Q5: [C to RTL design]**[40 points]**

The following C-code computes the intensity histogram of a series of pixel values while keeping track of the largest intensity count.

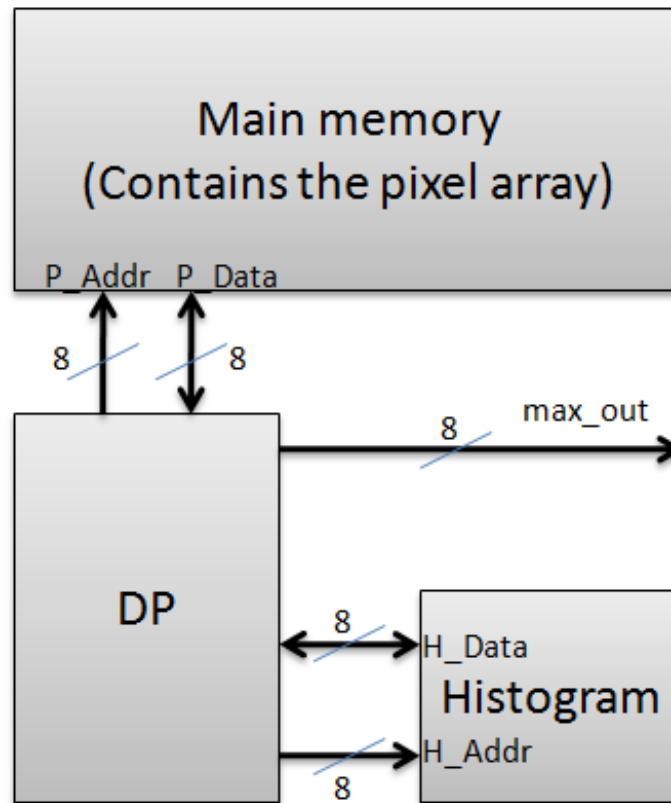
Inputs: byte pixels[256], bit start

Outputs: byte max_out, bit done

```
main() {  
    byte max;  
    byte pvalue;  
    byte hvalue;  
    byte i;  
    byte histogram[256]; // assume when cleared, all entries are set to 0  
  
    while(1) {  
  
        while(!start); // wait for start signal  
  
        done = 0;  
        i=0;  
        max = 0;  
        pvalue = 0;  
        hvalue = 0;  
  
        while(i<256) {  
            // for simplicity the following lines are split statements  
            // from histogram[pixel[i]]++;  
  
            pvalue = pixel[i];  
            hvalue = histogram[pvalue];  
            hvalue++;  
            histogram[pvalue] = hvalue;  
            if(hvalue>max) max = hvalue;  
            i++;  
        }  
  
        max_out=max;  
        done=1;  
    }  
}
```

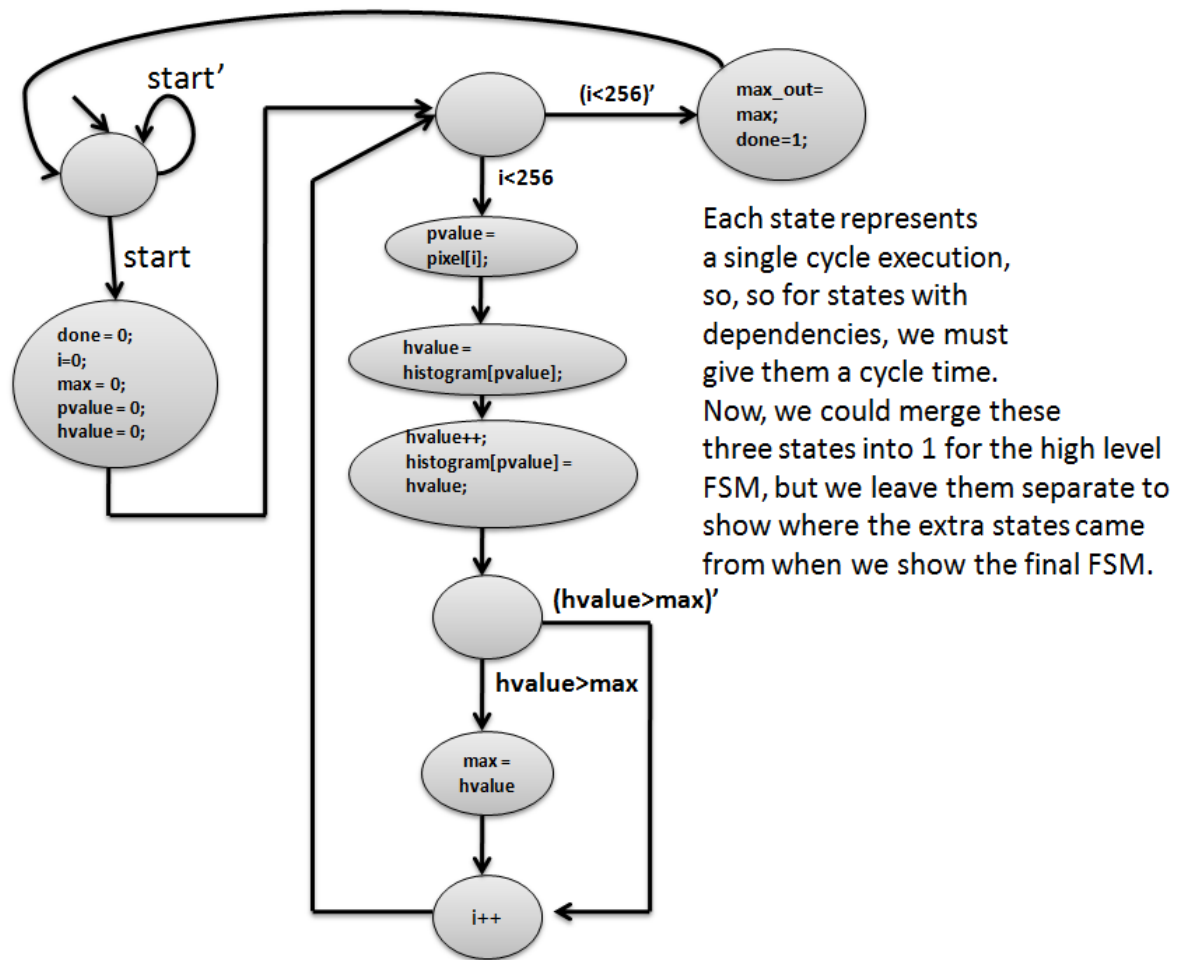
Student ID: _____

To help you understand, below is a block diagram of the datapath. It consists of the datapath black box, and two memory interfaces, the histogram memory (256 bytes), and main memory which contains the pixel array.



Student ID: _____

5a. Derive the high-level state machine from the provided C-code. [5 points]

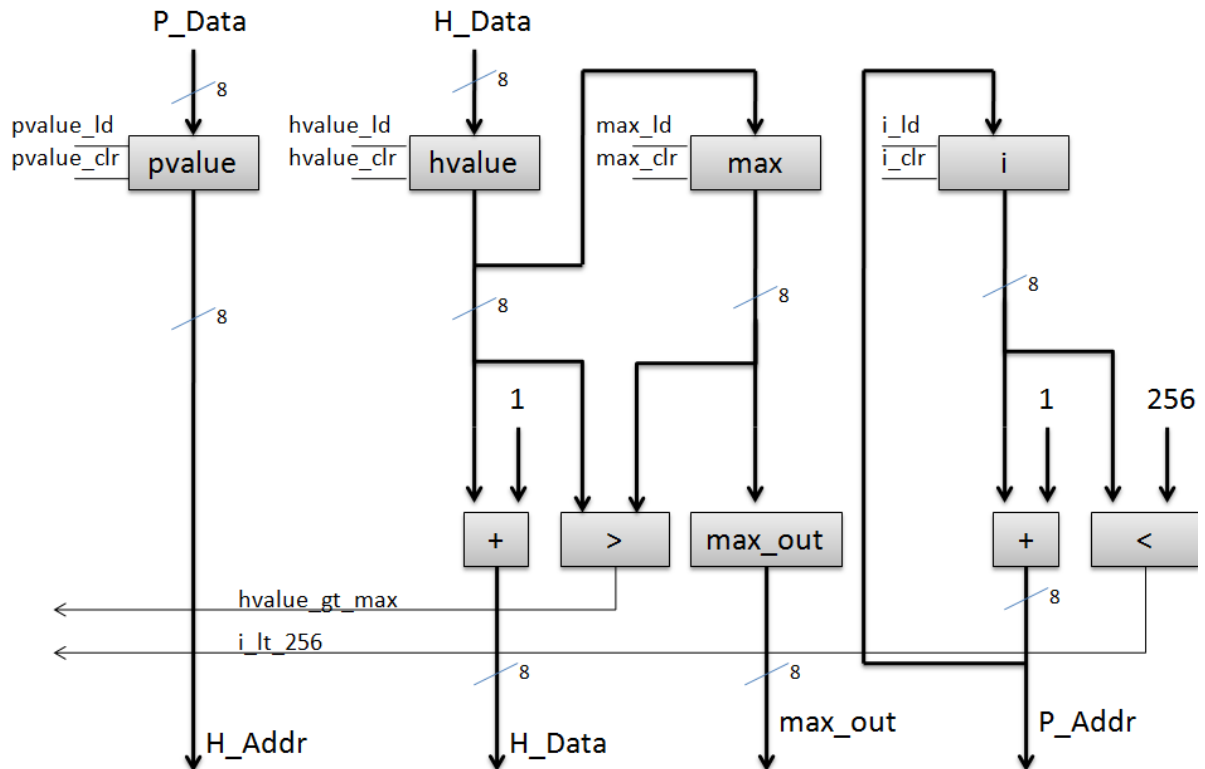


Student ID: _____

5b. Design the data-path for this system. [15 points]

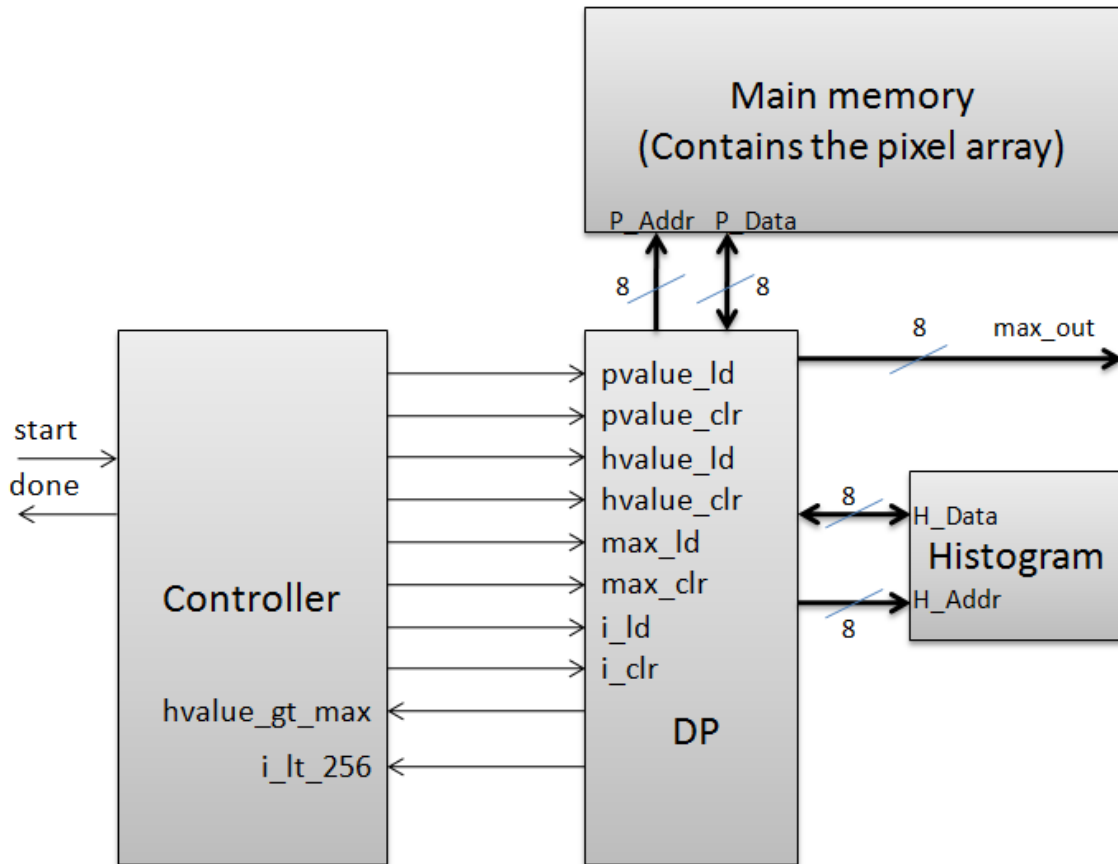
You may use any of the following components:

- 1) Registers
- 2) Adders
- 3) Comparators
- 4) Multiplexers



Student ID: _____

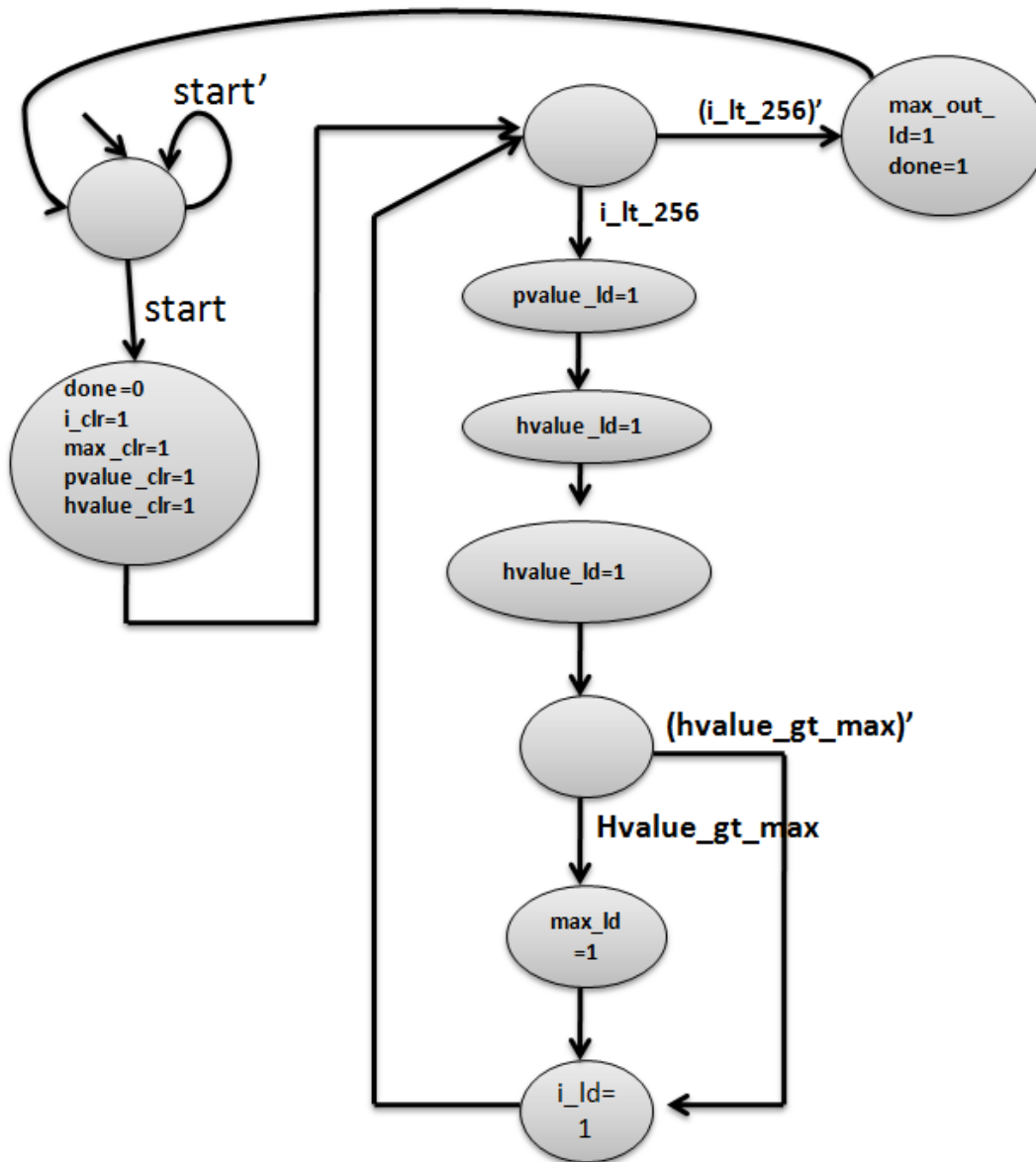
5c. Design the interface of the system and the interface between the controller and the datapath. [5 points]



Student ID: _____

5d. Design the FSM of the controller. [15 points]

HINT: There is no timing issue for this system so you do not have to consider timing issues in designing the controller's FSM.



Student ID: _____

<This page is intentionally left blank>

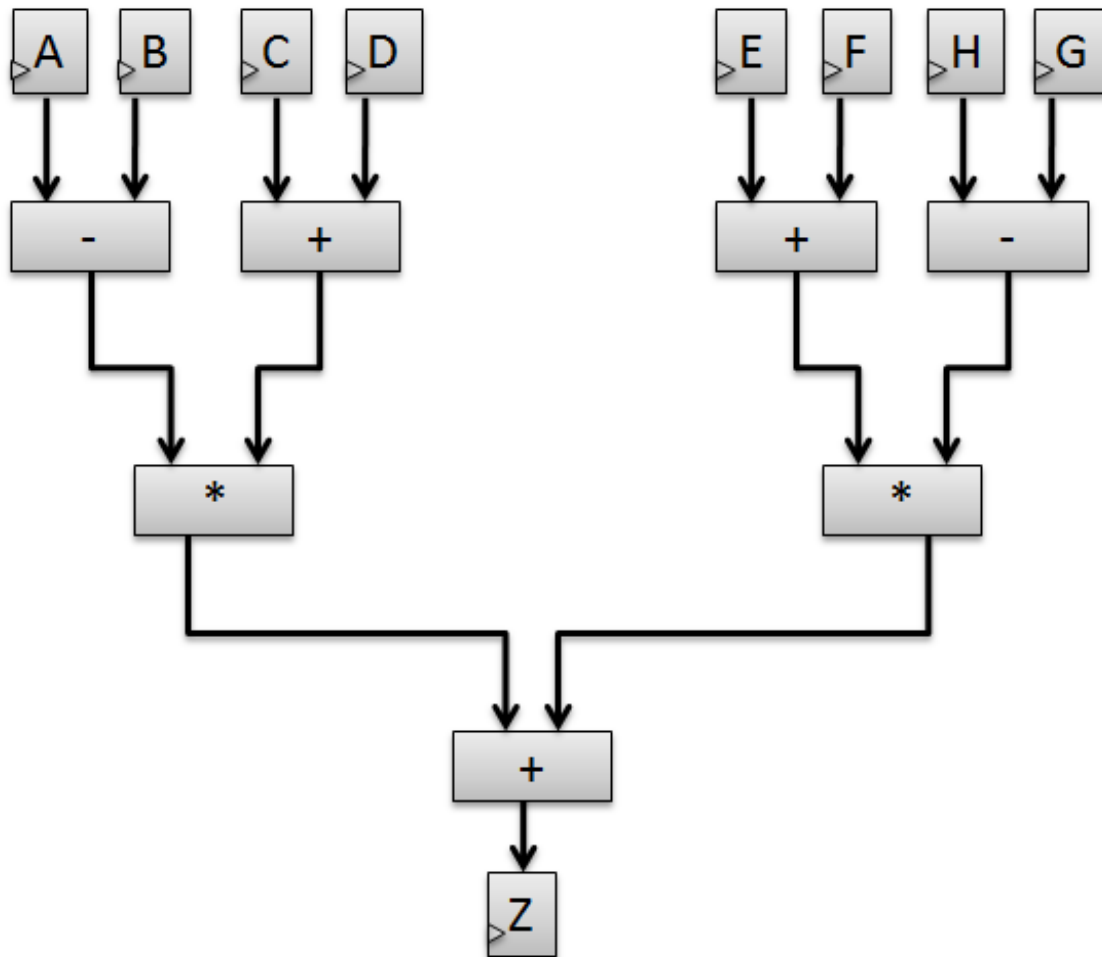
Question 6 [Pipeline utilization]

[20 points]

6a. Using only Adders, Subtractors, and Multipliers, design a circuit that performs the following operation: [5 point]

$$Z = (A-B)*(C+D) + (E+F)*(H-G)$$

A, B, C, D, E, F, G, H and Z are 8 bit registers.

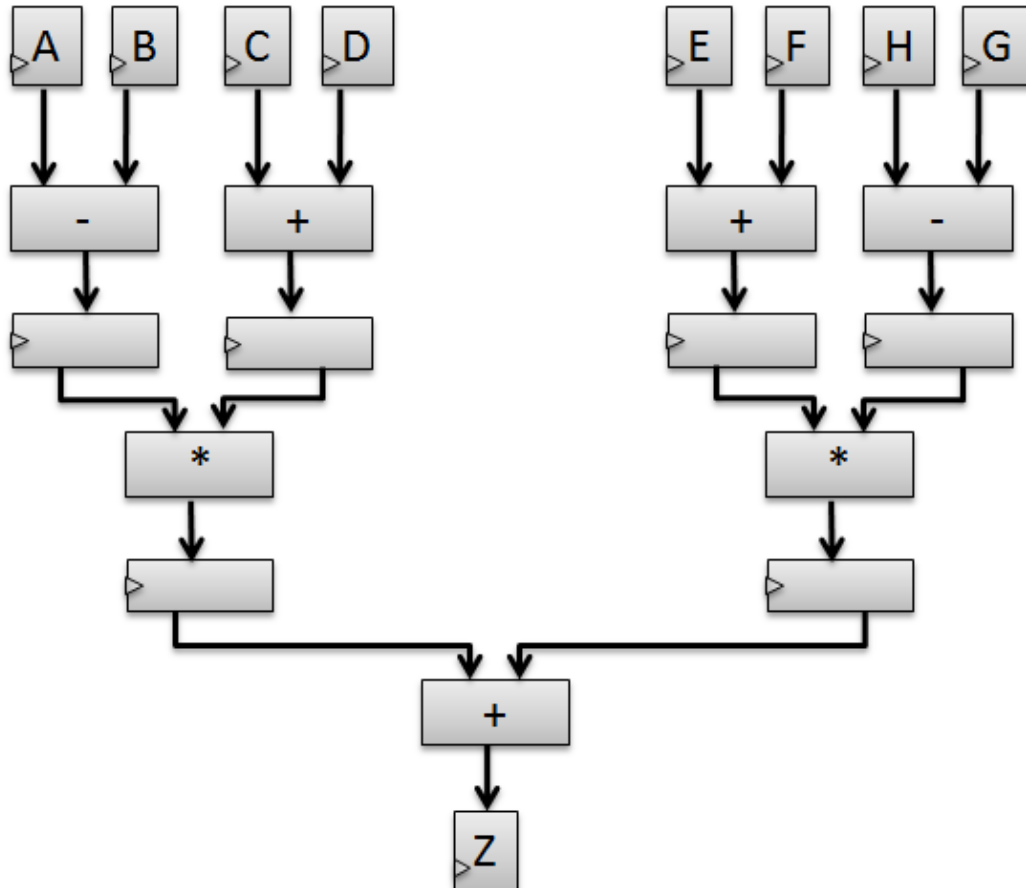


6b. If addition/subtraction takes 10 ns and multiplication takes 30 ns, what is the maximum allowed clock frequency for the above circuit? [5 points]

$$1 / (10\text{ns} + 30\text{ns} + 10\text{ns}) = 1 / (50 \text{ ns}) = 1000/50 \text{ MHz} = 20\text{Mhz}$$

Student ID: _____

6c. Add pipeline registers to your design in part (a) to make your design as fast as possible. [5 points]



6d. If addition/subtraction takes 10 ns and multiplication takes 30 ns, what is the maximum allowed clock frequency for the above circuit? [5 points]

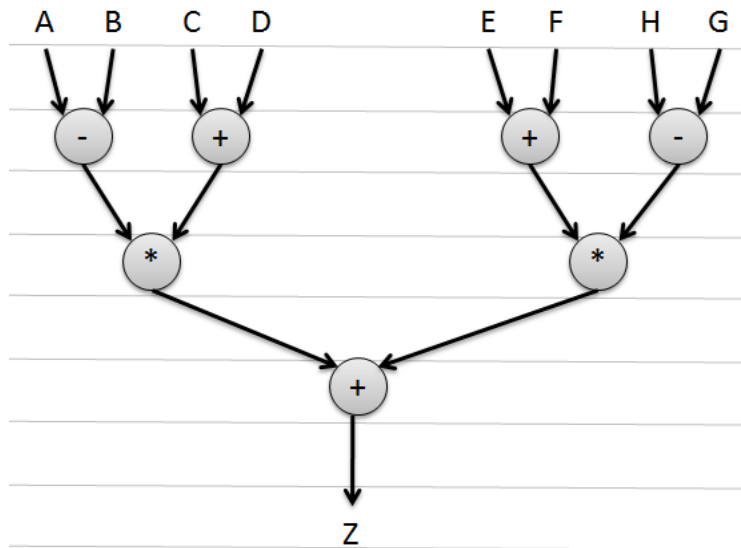
Longest register-to-register delay = 30ns

Frequency = $1 / (30\text{ns}) = 1000/30 \text{ MHz} = 100/3 \text{ MHz} = 33.3 \text{ MHz}$

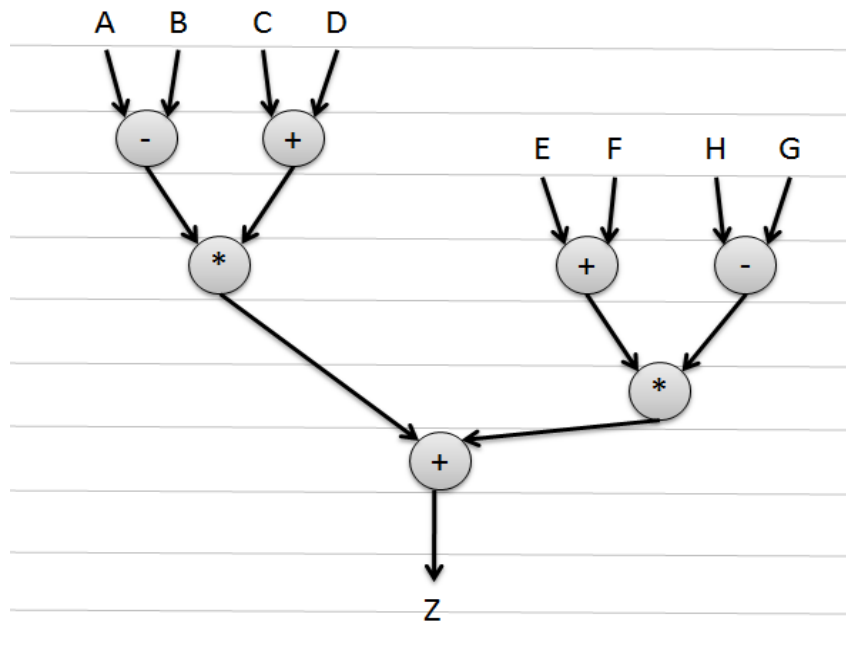
Student ID: _____

EXTRA CREDIT

E1: Consider the schedule below for computing $Z = (A-B)*(C+D) + (E+F)*(H-G)$ that uses 5 adder/subtractors and 2 multipliers:



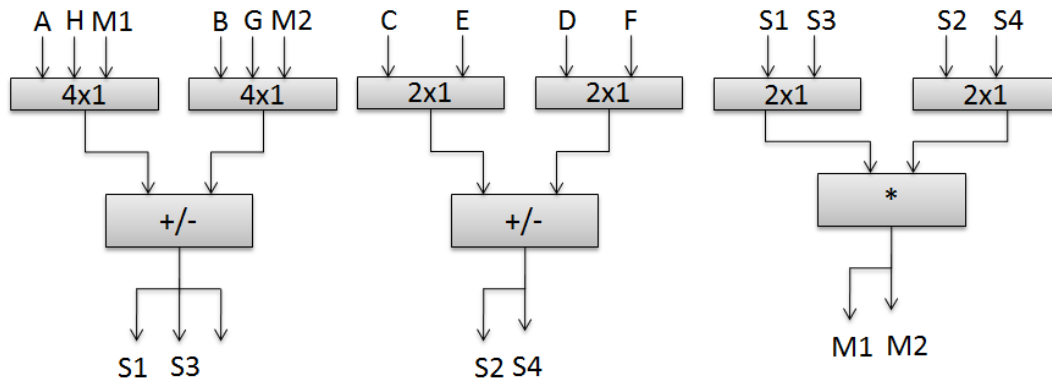
A. Draw a new schedule that uses only 2 add/sub modules and 1 multiplier. How many cycles it will take to compute a new value for Z? [5 points]



It will take 4 cycles, 1 cycle more than the original problem.

Student ID: _____

B. Draw the new datapath based on the schedule in part (e) [Hint: Add the required multiplexers] [5 points]



S1= A-B
S2=C+D
S3=H-G
S4=E+F
M1=S1*S2
M2=S3*S4