5.44

7	6	5	4	3	2	1	0	value
-	-	- r	E	D	C	B	A f	-
-	-	- r	E	D	C	B f	-	A
-	-	- r	E	D	C f	-	-	B
W	V	U	E	D	C fr	Y	X	-
W	V	U	E	D f	- r	Y	X	C
W	V	U	E	D fr	Z	Y	X	-
W	V	U	E f	- r	Z	Y	X	D
W	V	U f	-	- r	Z	Y	X	E
W	V f	-	-	- r	Z	Y	X	U

5.45

assume that both of wr and rd cannot be 1 at the same time.

Inputs : wr, rd, reset, eq

Outputs : rwr(register write), rrd(register read), rinc(rear inc), finc(front inc), full, empty, clr(register clear)

Outputs of each states; if not specified, they are 0

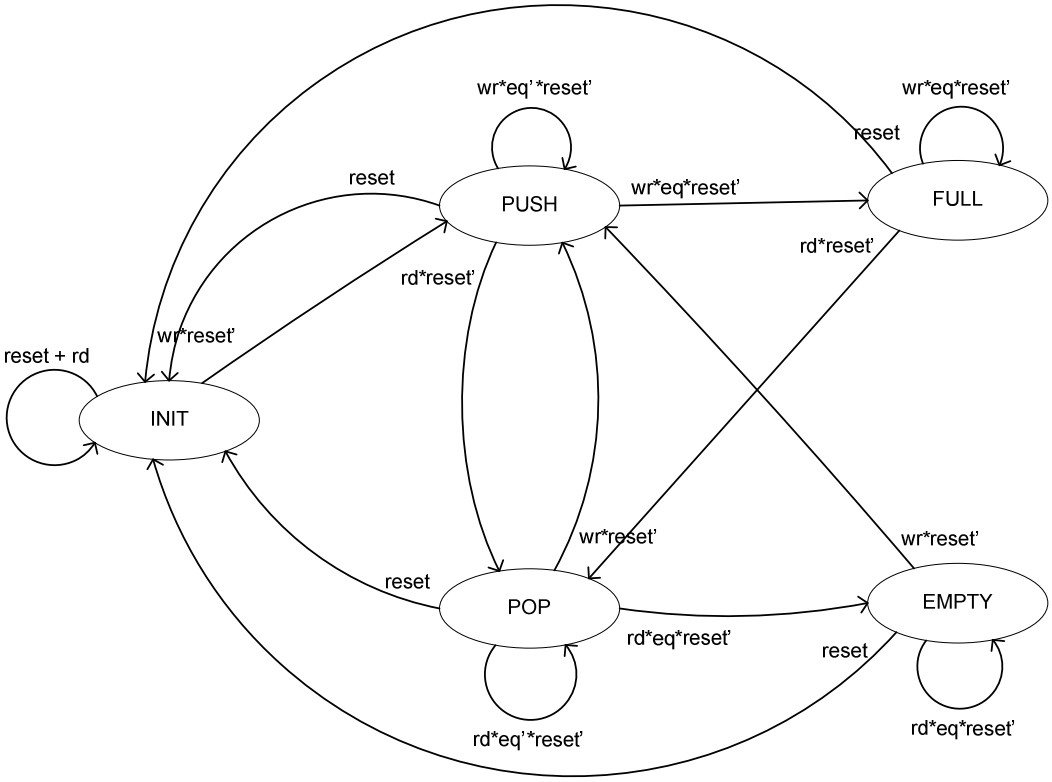
INIT : clr = 0

PUSH : rwr = 1, rinc = 1

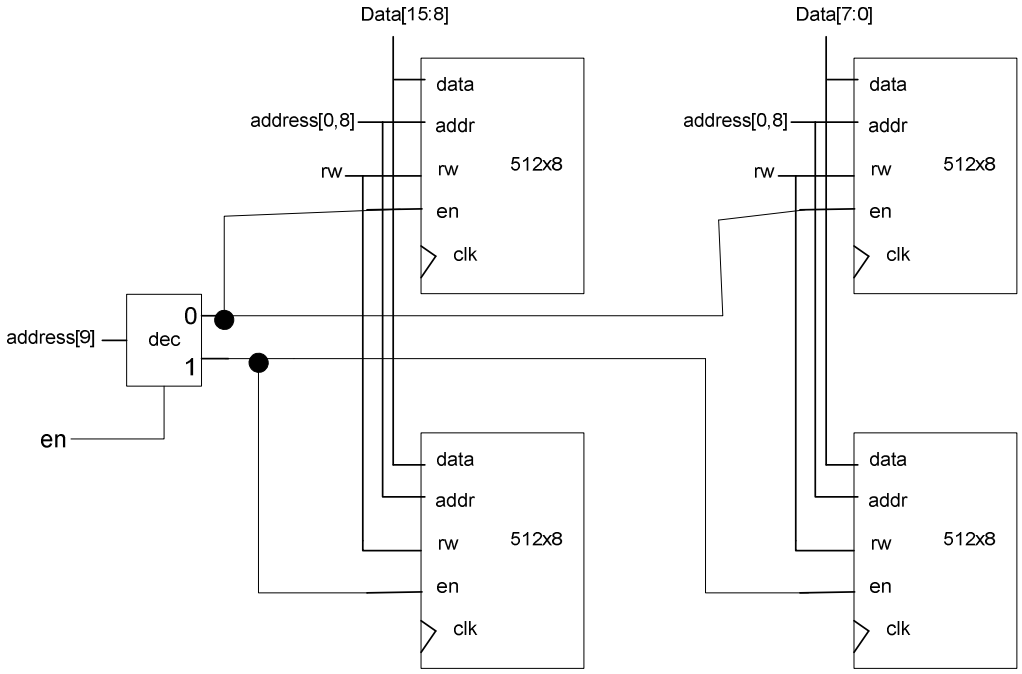
POP : rrd = 1, finc = 1

FULL : full = 1

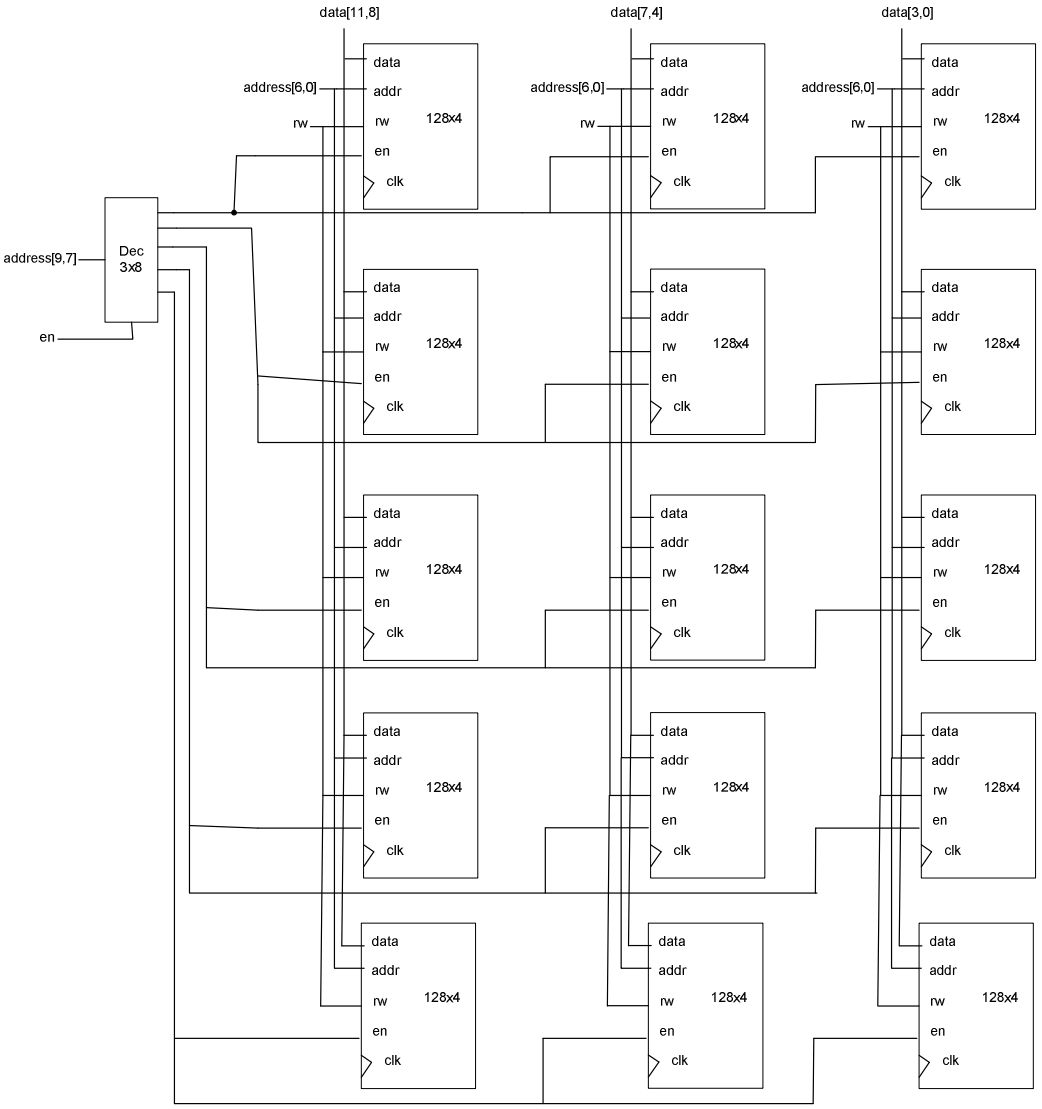
EMPTY : empty = 1



5.54


Data[15:8]
Data[7:0]
data
addr
rw
en
clk
512x8
address[0,8]
address[9]
dec
0
1
en

5.56


data[11,8]
data[7,4]
data[3,0]
address[6,0]
rw
address[9,7]
Dec
3x8
en
data
addr
rw
en
clk
128x4