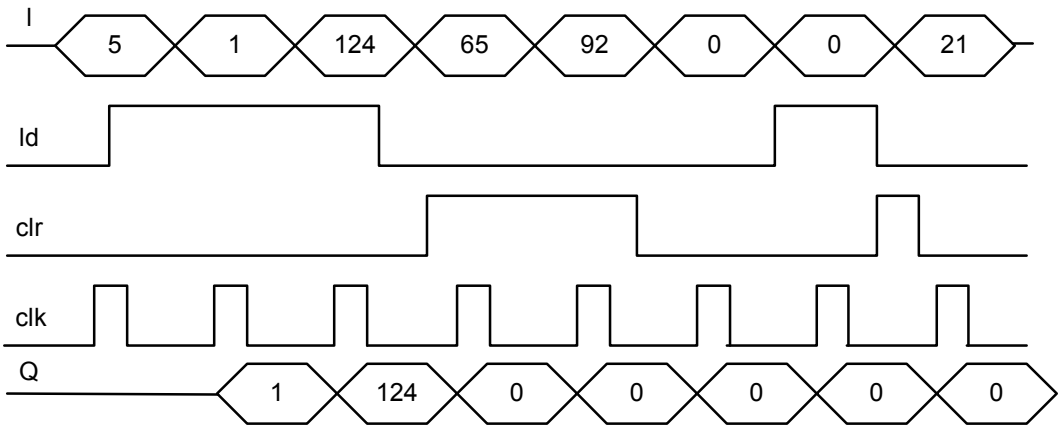
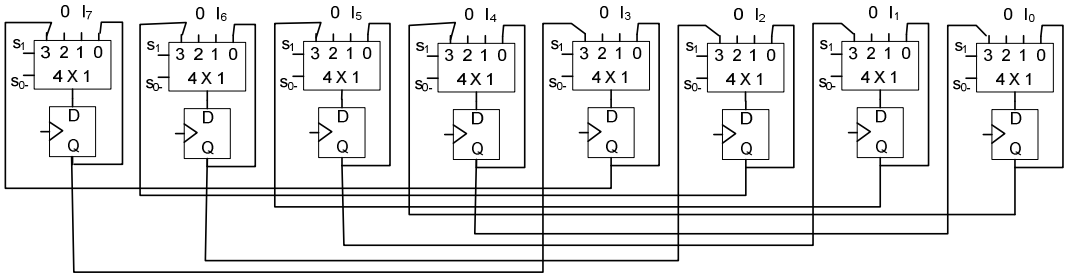
4.2



4.5

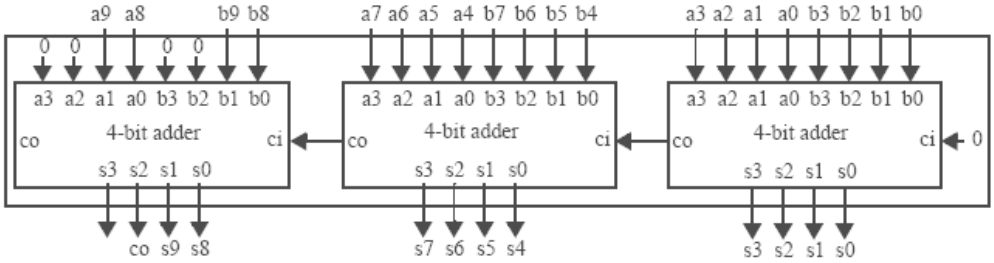


4.8

An 8-bit carry-ripple adder contains 7 full adders and 1 half adder. Each full adder requires 2 gate delays and the half adder requires 1 gate delay. Therefore a minimum of (7 FA * 2 gate delay/FA * + 1 HA * 1 gate delay/HA) * 1ns/gate delay = 15ns is required to ensure that the carry-ripple adder's sum is correct.

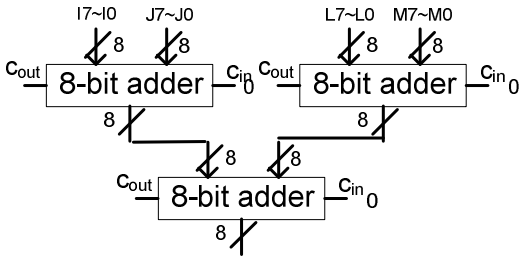
4.10

10-bit carry ripple adder

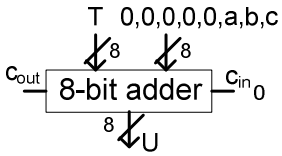


4.12

A+B+C+D = ((A+B) + (C+D))

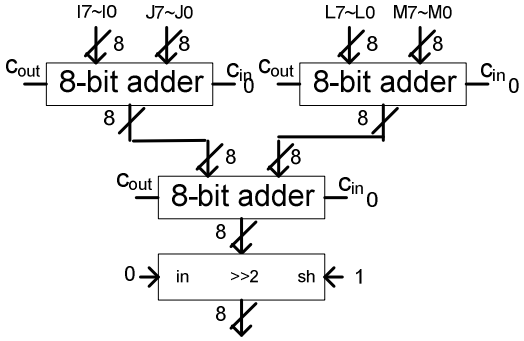


4.13

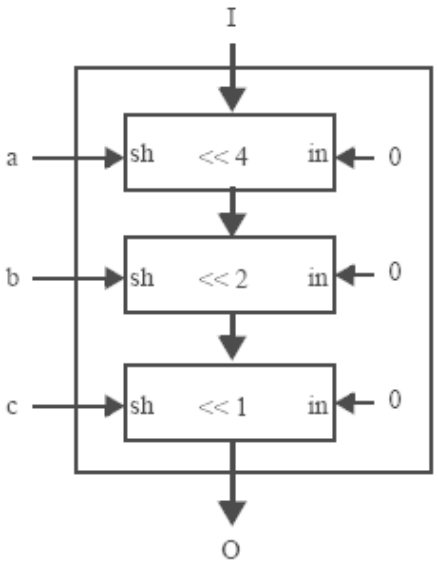


4.17

‘Divide by four’ means 2 right shifts in binary system.



4.20



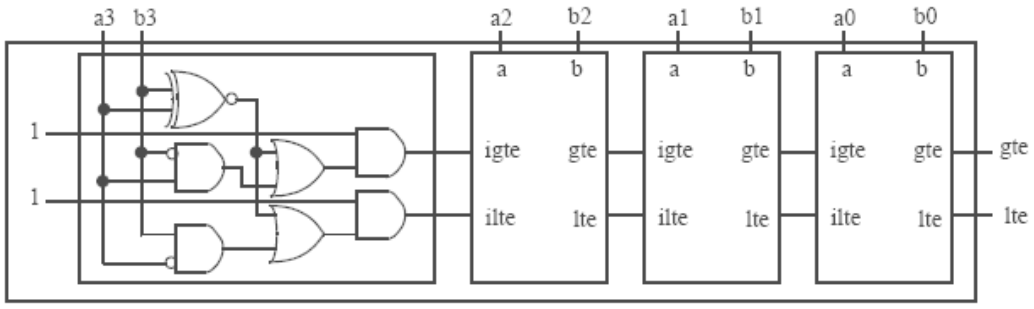
4.26

For each 1-bit comparator, assuming gte means “a is gte b” and lte means “a is lte b”,

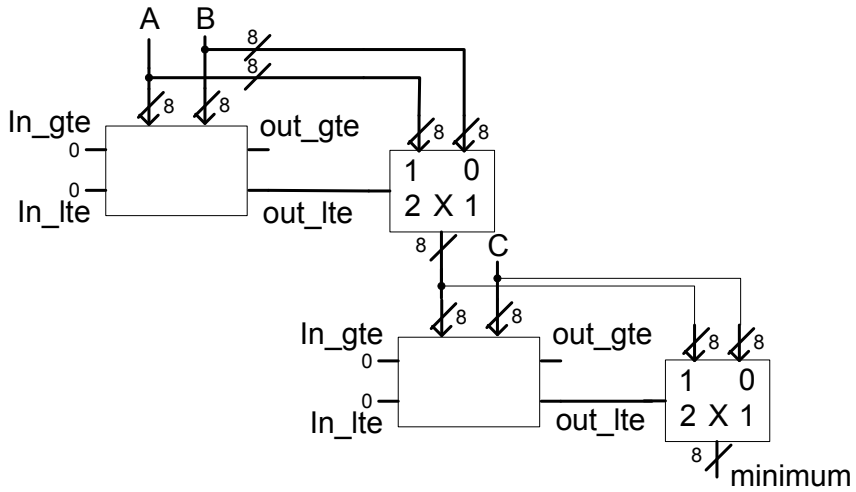
gte = igte((a XNOR b) + ab’),

lte = ilte((a XNOR b) + a’b).

“igte” and “ilte” are the result of comparison for higher bits:



4.29



4.48

(d) 11000000 → 2' complement 01000000 = 2^6 = 64

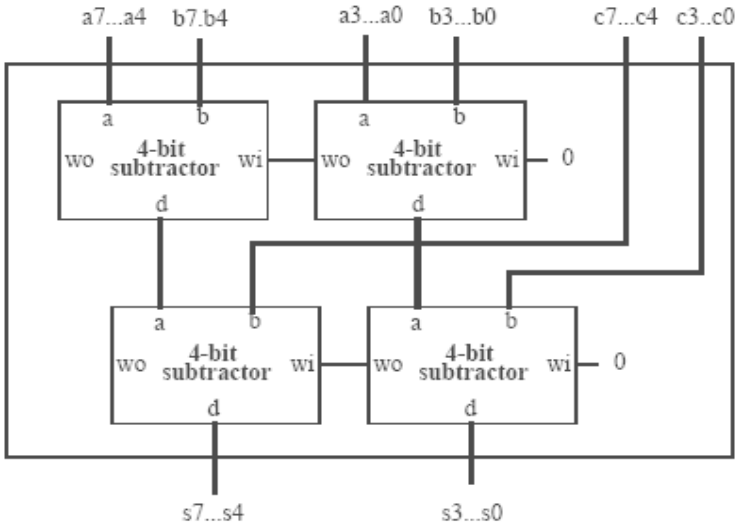
$(11000000)_2$ = -64

4.51

(f) 125 = 128 – 3 = 2^7 – 3 = 010000000 – 011 = 01111101

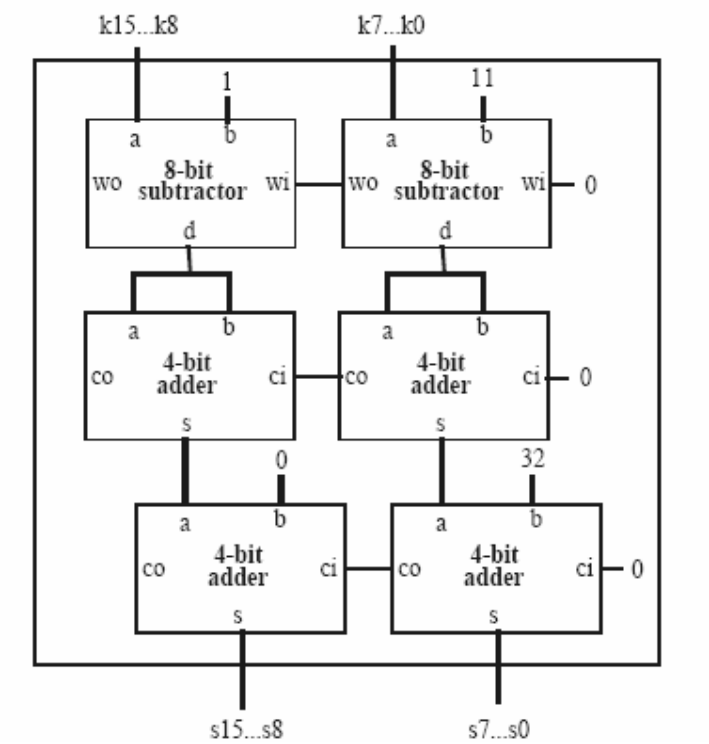
Therefore, -125 is 10000011 in two's complement form

4.54

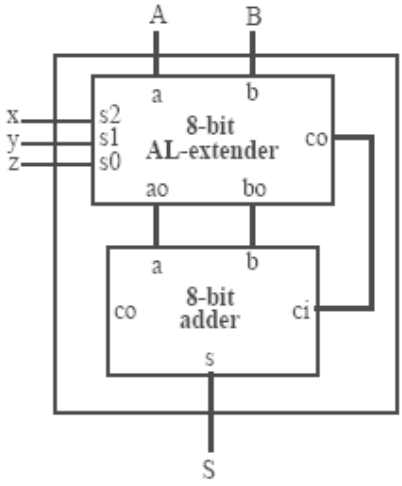


4.55

$(273)_{10} = (111)_{16}$



4.56



Operation of the AL-extender:

When xyz=000, ao=a, bo=b', co=1

When xyz=001, ao=a, bo=b, co=0

When xyz=010, ao=a<<3, bo=0, co=0

When xyz=011, ao=a>>3, bo=0, co=0

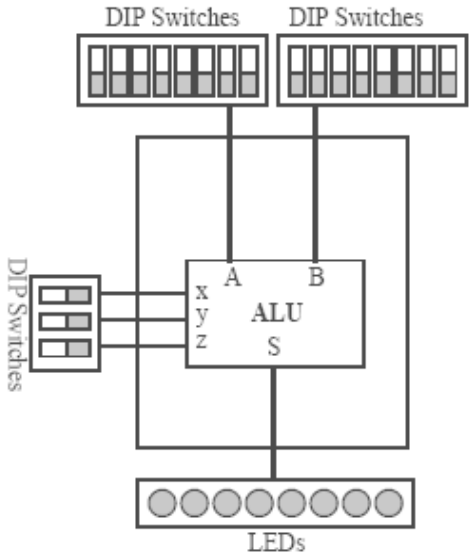
When xyz=100, ao=a NAND b, bo=0, co=0

When xyz=101, ao=a XOR b, bo=0, co=0

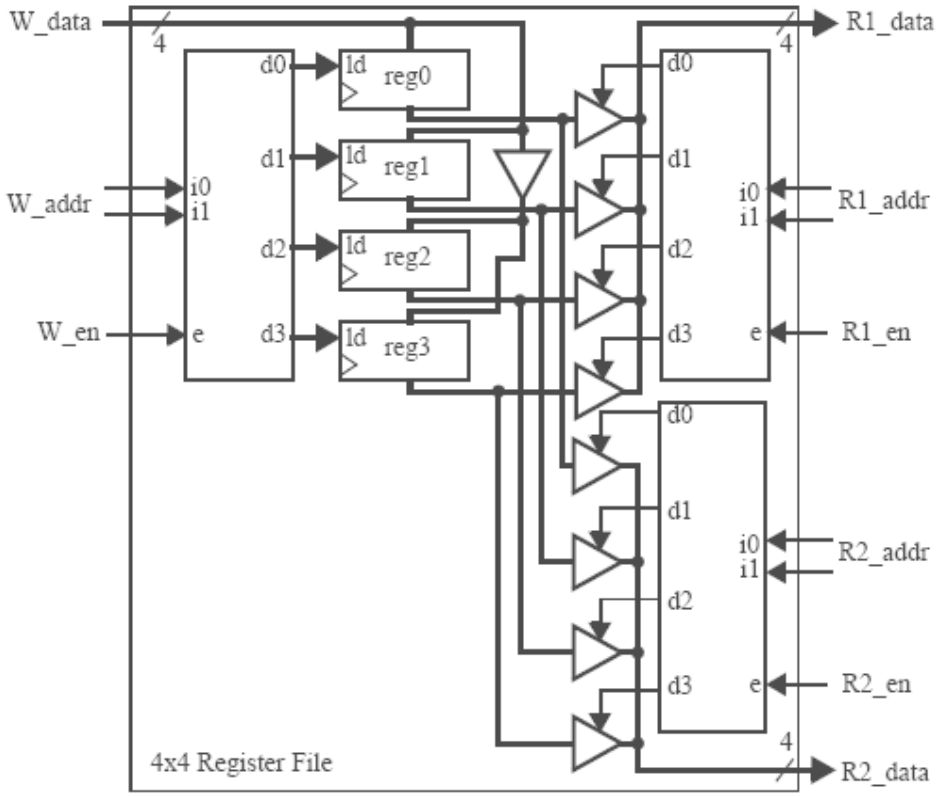
When xyz=111, ao=a reversed, bo=0, co=0

When xyz=111, ao=NOT a, bo=0, co=0

4.58


DIP Switches
DIP Switches
DIP Switches
A
B
x
y
z
ALU
S
LEDs

4.60


W_data
4
R1_data
4
d0
ld
reg0
d1
ld
reg1
d2
ld
reg2
d3
ld
reg3
W_addr
i0
i1
W_en
e
d0
d1
d2
d3
i0
i1
R1_addr
e
R1_en
d0
d1
d2
d3
i0
i1
R2_addr
e
R2_en
4
R2_data
4x4 Register File