Towards Soft Errors*

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Abstract

This document deals with the causes and effects of single energetic particle on advanced microelectronics called SEE (Single-Event Effects). SEE can be classified into hard errors such as SEL (Singl-Event Latchup) and SEB (Single-Event Burnout), and soft errors like SEU (Single-Event Upset) and SET (Single-Event Transient). Hard errors are permanent, i.e., they remains active permanently, so hardware redundancy such as Triple Modular Redundancy can recover them usually. On the other hand, soft errors can be tolerated by most redundancy techniques like temporal redundancy, data redundancy and software as well as hardware redundancy since resetting or rewriting the devices restores normal behavior thereafter. Transient faults (soft errors) are our main interests so this document focuses on the sources, mechanisms and trends with an advance of technology toward soft errors not only in memory but also in logic components.

1 Introduction

Technology scaling has been the primary engine for industry survival and is the driving factor for higher density, improved performance, and cost reduction. As device technology scales to deep-submicron gate lengths (0.25 microns to 90 nm and beyond), the cell size of memory products continues to decrease, thus driving the supply voltage lower (5 V to 3.3 V to 1.8 V and smaller) and reducing the capacitance inside the cell (10 to 5 fF [1] and smaller). Due to the lower capacitance, the critical charge, the minimum charge required for a cell to retain data, in memory devices continues to shrink, thereby decreasing their natural resistance to SEUs. Therefore, a low-energy alpha particle or a cosmic ray can disturb the cell more vulnerably with technology scaling [7].

Further, the sensitivity of random logic has been investigated recently and is becoming increasingly important since the susceptibilities of random logic and SRAM cells to alpha particle induced soft errors are very similar, and core logic SER (Soft Error Rate) is of the same order of magnitude for both neutrons and alpha particle hits [13, 15, 2].

SEUs are random and rarely catastrophic, and they do not normally destroy a device. Many systems can tolerate some level of soft errors. For example, if you are designing a precompression capture buffer or a postdecompression playback buffer for an audio-, video-, or still-imaging system, an occasional bad bit may be unnoticeable and unimportant to the user. However, when you use memory elements in mission-critical applications to control system functions, soft errors can have a more serious impact and lead to not only corrupt data, but also a loss of function and system-critical failures [7]. Compared to embedded systems, desktop processors now utilize large, high-density memories, which significantly increases the vulerability of systems to soft error failure. Embedded systems, such as those utilized in portable and wireless products, are generally more tolerant since they contain less memory and use processors designed to operate at lower clock speeds than PC systems. However, they are more likely to be used in safety-critical systems and consumer products where reliability is important. In addition, embedded processor manufacturers are increasingly turning to the latest technologies to achieve low power and reduced cost advantages, leading them to confront the soft error challenge too [11].

2 Single-Event Effects (SEE)

The natural space environment contains several subatomic energetic particles such as neutrons, protons and heavy ions that can collide with electronic devices and cause different types of damage. Single-Event Effects

*Many sentences of this document have been facsimiled and revised from references

[1] A capacitor has one value of farad (symbol: F) when one coulomb of charge causes a potential difference of one volt across it. 1 fF pronounced femtofarad equals 10^{-15} F.

(SEE) are disturbances in an active electronic device caused by a single, energetic particle and can take on many forms. They normally appear as transient pulses in logic or as bitflips in memory cells or registers. As semiconductor process geometries decrease, transistor threshold voltage also decreases. These lower thresholds reduce the ionizing field charge per node required to cause errors thereby increasing the devices susceptibility to SEE [12]. Single event phenomena can be classfied into three effects in order of permanency as plotted in Figure 1:

1. Single-Event Upset (SEU)
2. Single-Event Latchup (SEL)
3. Single-Event Burnout (SEB)

SEU is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs" [9]. SEU reverses the stored digital information in a storage or sequential circuit. SEUs are transient and non-destructive soft errors, which means that a reset or rewriting of the device results in normal device behavior thereafter. SEUs manifest themselves as either SBUs (Single-Bit Upsets) or MBUs (Multiple-Bit Upsets). SBU refers to the flipping of one bit due to the passage of a single energetic radiation particle, where MBU is possible in which a single ion hits two or more bits causing simultaneous errors [7]. SER of MBUs is much less (hundreds or thousands of times less) than that of SBUs [6]. Another soft error is SET (Single-Event Transient), which occurs when a cosmic particle strikes a sensitive node within a combinational logic circuit. A voltage disturbance is produced at that node which may propagate through the logic.

SEL is a condition that causes loss of device functionality due to a single-event induced current state. These errors are hard errors and can cause permanent device damage. SEL results in a high operating current, above device specification. If power is not removed quickly, catastrophic failure may occur due to excessive heating, metalization or bond wire failure [3, 4, 16, 9].

SEB is a condition that can cause device destruction permanently due to a high current state in a power transistor. SEBs include burnout of power MOSFETs (Metal Oxide Silicon Field Effect Transistors), gate rupture, frozen bits, and noise in CCDs (Charge-Coupled Devices) [3, 4, 16, 9].

This document concentrates on soft errors, i.e., transient faults, since hard errors or permanent faults like SEL and SEB are beyond our interests.

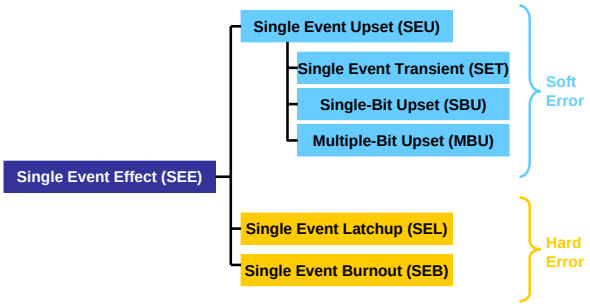

Figure 1. Classfication of Single Event Effects.

3 Soft Errors - Single-Event Upsets (SEU)

SEUs are soft errors, i.e., transient faults or bitflips, caused by an energetic particle. They are temporary and non-recurring since a reset of the device results in normal device behavior. In other words, after observing a soft error, there is no implication that the system is less reliable than before. External radiation induces SEUs predominantly and intrinsic noise as well as interference can also cause SEUs; but they can be accommodated by design engineers. Three main sources to soft errors are alpha particles, cosmic rays and thermal neutron. Thermal neutrons are primarily an SEU issue only if BPSG (Boron-Phosphor-Silicate-Glass) dielectric layers are present; eliminating the use of B-10 isotopes effectively addresses the problem [7].

3.1 Soft Error Rate (SER)

The rate at which SEUs occur is given as SER, and you measure it in FITs (Failures in Time), which expresses the number of failures in one billion device-operation hours. A measurement of 1,000 FITs corresponds to a MTTF (Mean Time To Failure) of approximately 114 years [2]. The potential impact on typical memory applications illustrates the importance of considering soft erros. A cell phone with one 4 Mbit, low-power memory with an SER of 1,000 FITs per megabit will likely have a soft error every 28 years. But a high-end router with 10 Gbits of SRAM and an SER of 600 FITs per megabit can experience an error every 170 hours. For a router farm that uses 100 Gbits of memory, a potential networking error interrupting its proper operation could occur every 17 hours. Finally, consider a person on an airplane over the Atlantic at 35,000 feet working on a laptop

[2] $10^9/(1,000 * 24 * 365) = 114.16$

with 256 Mbytes (2 Gbits) of memory. At this altitude, the SER of 600 FITs per megabit becomes 100,000 FITs per megabit, resulting in a potential error every five hours. The FIT rate of soft errors is more than 10 times the typical FIT rate for a hard reliability failure. Soft errors are not the same concern for cell phones as they can be for systems using a large amount of memory.

3.2 Soft Errors from Alpha Particles

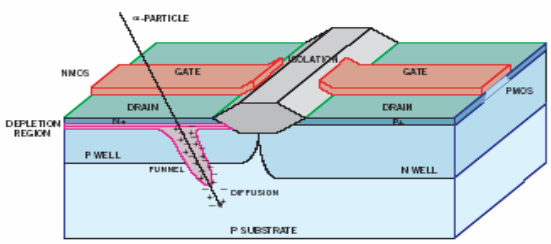

Figure 2. The alpha particle generates electron-hole pairs in its wake, causing the charges to drift so that the transistor sees a current disburbance [7].

Alpha particle-induced soft erros refer to transient errors in the operation of a dynamic random acess memory (DRAM) devices caused by alpha particles emitted by traces of radioactive elements such as uranium and thorium present in the packaging material of the device like ceramic packages and lead-based connectors. These alpha particles manage to penetrate the die and generate a high density of holes and electrons in its substrate as displayed in Figure 2, which creates an imbalance in the device's electrical potential distribution that causes stored data to be corrupted. The alpha particles emitted by the device package can have energies of 2 to 9 MeV (Million electron Volt). It takes about 3.6 eV to generate an electron-hole pair in the substrate, so an alpha particle can generate approximately one million electron-hole paris within 2 to 3 microns of the alpha particle track. The potential well of a memory cell that contains a '0' is filled with electrons (inversion mode), while that of a memory cell that contains a '1' is devoid of electrons (depletion mode). When an alpha particle hits the substrate and generates holes and electrons, the holes will be pulled toward the substrate supply while the electrons will be pulled toward the potential well. An empty well can fill up with enough electrons to have its stored information reversed from '1' to '0'. Cells that already have electron-filled wells in the first place are not affected by alpha particles. The amount of charge needed to corrupt stored information and result in a soft error is referred to as the critical charge, or Q_{crit}. Q_{crit} becomes smaller as devices are reduced in size and operating voltages, making soft errors bigger problem for smaller devices. Q_{crit} is also a function of the stored charge in the memory cell. Alpha particles normally cause SBUs because they have lower energies, but they can cause MBUs in devices with low supply voltage. Soft error rates due to alpha particles may be minimized by: 1) reducing the number of alpha particles emitted by the package; 2) coating the chip surface with a film such as polyimide resin that blocks alpha particle irradiation; and 3) better design of memory device to make it less sensitive to alpha-induced soft errors.

3.3 Soft Errors from Cosmic Rays

Heavy ions of cosmic rays cause a direct ionization SEE, i.e., if an ion particle transversing a device deposits sufficient charge, an event such as a memory bit flip or transient may occur. Cosmic rays may be galactic or solar in origin as shown in Figure 3.

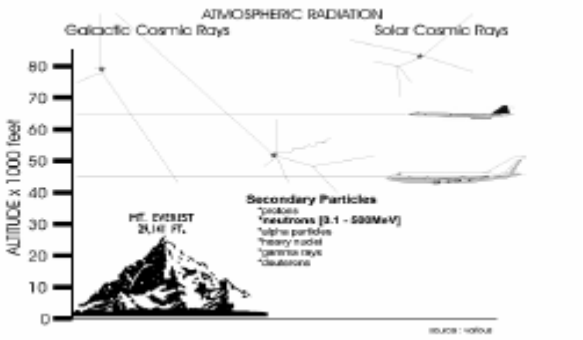

Figure 3. Atmospheric Radiation Environment [12].

Protons, usually trapped in the earth's radiation belts or from solar flames, may cause direct ionization SEEs in very sensitive devices. However, a proton may more typically cause a nuclear reaction near a sensitive device area, and thus, create an indirect ionization effect potentially causing an SEE. High-energy neutrons have energies of 10 to 800 MeV; in contrast, protons have energies greater than 30 MeV. High-energy neutrons have no charge; therefore, they do not coulombically interact with the semiconductor material, so their interaction with silicon differs from that of an alpha particle. High-energy neutron produces ionized particles by colliding with the silicon nucleus and undergoing impact ionization with the silicon nuclei. This collision can generate alpha particles and other heavier ions, thus producing electron-hole pairs but with higher energies than a typical alpha particle from mold components [12, 7, 3, 16].

The schematics in Figure 4 show how galactic cosmic rays deposit energy in an electronic device. And shielding is ineffective against galactic cosmic rays due to their high energyies [4]. Neutrons are in particular troublesome, since they can penetrate most manmade construction [7]. A neutron, for instance, can pass through five feet of concrete. The flux-rate is geoposition-dependent and increases at higher altitudes due to a lower shielding effect of atmosphere. For example, the effect in London is 1.2 times worse than at the equator. In Denver with its high altitude, the effect is three times worse than at sea level in San Francisco. In an airplane, the effect can be 100 to 800 times worse than on the ground [7].

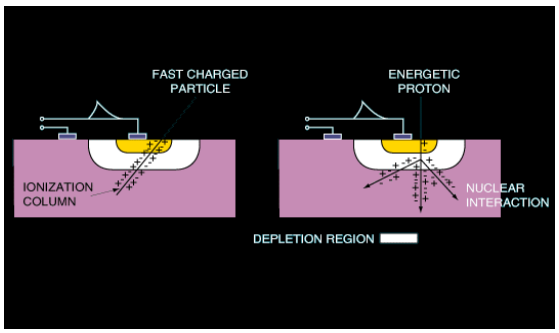

Figure 4. Effects of cosmic rays on an electronic device [4]. Original source is *"Spacecraft Anomalies due to Radiation Environment in Space" by Lauriente and Vampola.*

3.4 SER Scaling Trend

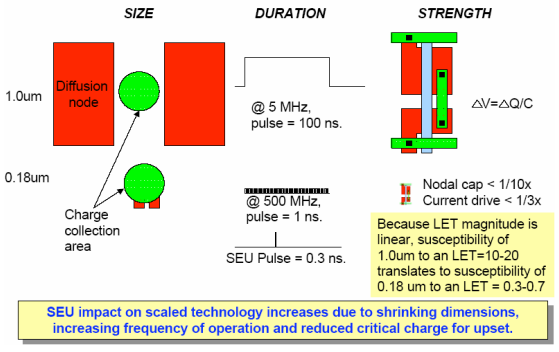

Figure 5. Effects of scaling on SEU [3].

The SER problem first gained widespread attention as a memory-data issue in the late 1970s, since DRAMs began to show signs of random failures. As process technologies continue to shrink, the critical charge required to cause an upset is decreasing faster than the charge-collection area in the memory cell. Therefore, with smaller geometries, such as 90 nm, soft errors are more of a concern, and designers must take steps to control SER levels [7]. The effects of scaling on SEUs are explained in the Figure 5. Shrinking demensions, increasing frequency of operation and reduced critical charge for upset increase SEU with an advance of scaled technology.

3.4.1 SER Trend in DRAM

Historically, DRAM devices had poor SER due to their small stored charge versus their large collection cross-section for funneling charge created by alpha particles or cosmic rays. SER of DRAM is smaller than that of SRAM, i.e., DRAMs are much more immune to soft error than SRAMs in current technology. For example, SER in 1T-DRAM is more than 10 times better than 6T SRAM. Figure 6 shows industry trend on DRAM SER over many process generations, which illustrates that the DRAM single bit SER has been reduced by about four to five times per generation. This continuous reduction is attributed to the shrinking junction volumes (lowering the collected charge), the relatively high node capacitance (achieved with an external three-dimensional cell capacitor), and the relatively gradual voltage scaling [1]. [5] discusses this reduction and concludes that DRAM devices generally have improved SER with each new process generation due to the faster reduction of collection cross-section as compared to critical charge reduction. There is some concern [14] that as DRAM density increases further and thus the components on DRAM chips get smaller, whilst at the same time operating voltages continue to fall, DRAM chips will be affected by such radiation more frequently since lower energy particles will be able to change a memory cell's state. On the other hand, smaller cells make smaller targets, and moves to technologies such as SOI (Silicon On Insulator) may make individual cells less susceptible and so counteract, or even reverse this trend. As shown in Figure 6, DRAM failure rates at the system level, however, have remained unchanged because system memory size has increased as fast as the reduction in single bit SER [1]. Today's DRAM devices typically have SER in the order of a few hundred to a few thousand failures in a billion device hours (FITs) when operated at full speed [16].

3.4.2 SER Trend in SRAM

Six transistor SRAM (6T SRAM) devices traditionally had superior SER immunity due to high signal levels from high operating voltages and their more stable cell made up of two large cross-coupled inverters, each strongly driving the

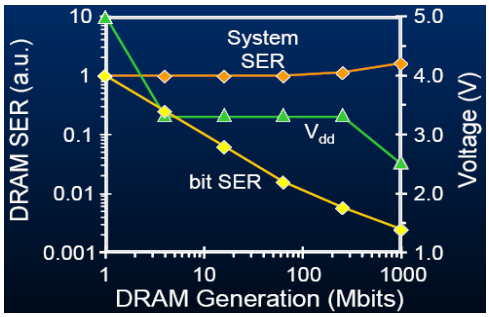

Figure 6. DRAM SER scaling trend [1, 2].

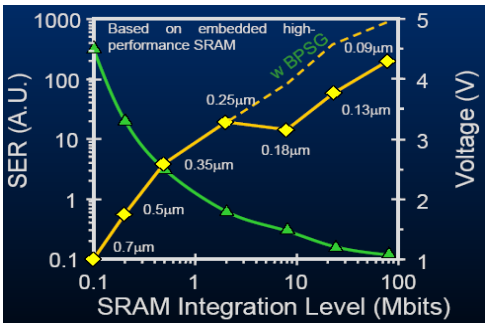

Figure 7. SRAM SER scaling trend [1, 2].

other to keep the bit in its programmed state [5, 1]. However, SRAM devices tend to have worsening SER with each new process generation due to the faster reduction of critical charge required to cause an error as compared to collection cross-section reduction [5], with the degradation factor of 5 to 10 times for each new process generation as plotted in Figure 7. [1] explains this trend with the intuitions that reductions in cell collection efficiency, with each successive SRAM generation, due to the shrinking cell depletion volume have been swamped out by big reductions in operating voltage and reductions in node capacitance. Thus SRAM single bit SER increased with each successive generation, particularly in products using BPSG. Most recently, as feature sizes have been reduced into the deep sub-micron regime, the SRAM single bit SER is due to saturation in the voltgae scaling (further reduction in operating voltage is limited by transistor threshold voltages), reductions in junction collection efficiency, and increased charge sharing due to short-channel effects with neighboring nodes. The exponential growth in the amount of embedded SRAM in electronics had led the SRAM system SER to increase with each generation. Six-transistor SRAMs in current process geometries are already approaching several hundreds FITs and are expected to increase to approximately 10,000 FITs at the 0.15 micron generation and 50,000 to 100,000 FITs at 0.13 micron generation when operated at full speed [5, 16]. On the other hand, Flash memory is much more immune to soft errors than SRAMs and DRAMs [10].

3.4.3 SER Trend in Logic Components

In general, soft errors within logic circuits are viewed as less of a threat to circuit malfunction. Since sequential logic elements are less densely packed, they are statistically less likely to be affected by particle collisions than larger memory areas [11]. Thus, SER has been focused traditionally on random access memory such as SRAM and DRAM but recent literatures investigate the effects of soft errors on logic components like a processor core, which are becoming increasingly important as simulated in Figure 8. The core of modern electronic systems consists of a microprocessor or digital signal processor with a large embedded memory (usually SRAM) interconnected by sequential logic. Such systems usually incorporate a large external memory (typically DRAM). These logic elements include latches and flop-flops used to hold system event signals and buffer data before it goes in or out of the chip – combinatorial elements that perform logical operations based on multiple inputs can also contribute to the chip SER (if the transient error that is induced by radiation is latched in a flip-flop or latch) but were not considered seriously. Flip-flops and latches are similar to SRAM cells in that they use a cross-coupled inverters, however, they have historically been much more robust against soft errors because they are constructed with more and larger transistors which can more easily compensate for spurious charge collected during radiation events [1]. The results obtained from SER simulation of flip-flop and latch circuits for 0.18 and 0.13 micron technology nodes and from the preliminary alpha particle SER characterization of the 0.13 micron logic test structure are shown in Figure 8. This trend is disturbing since even at the 0.13 micron node SER in the sequential logic are high enough to limit the efficacy of memory error correction since the logic bit SER is only hundred to thousand times lower than SRAM bit SER, while the failure rate of EDAC (Error Detection And Correction) protected memory is at least ten times lower [1].

Figure 9 shows the estimated SER contributions of various elements for typical designs such as microprocessors, network processors, and network storage controllers [8]. The SER contribution of combinational logic for state-of-the-art processes is still considerably smaller compared to the contributions of unprotected SRAMs and sequential elements such as latches and flip-flops. For core logic, asynchronous soft errors are much more common than synchronous ones [13]. The impact of operating frequency on the chip-level SER is therefore negligible. Further, it is significantly costly for core logic to tolerate faults since it re-

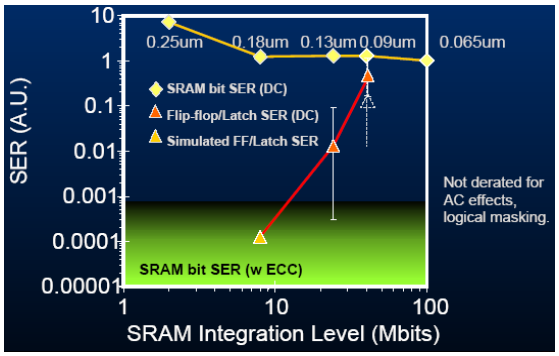

Figure 8. Logic SER trend [1, 2].

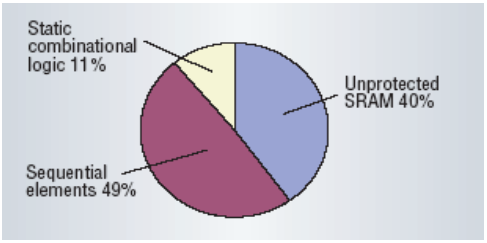

Figure 9. Contributions to the overall SER for a design manufactured using state-of-the-art technology [8].

quires more logic and redundancy driving the logic complex while ECC (Error Correction Coding) is common to tolerate the soft error in memory. The detection and protection of areas of a microprocessor from the effects of soft errors is difficult; available solutions often incur significant penalities in area and performance and are still not always 100 percent effective in resolving soft errors. Even when a solution delivers the anticipated error detection facilities, error correction remains hugely complex. For example, Mitigation of soft errors in logic involves the use of multiple identical logic paths feeding into a majority voting circuit. This method uses three times the chip area and reduces maximum operating frequencies since extra gate delays are introduced. More importantly this type of intervention, because it is so costly, requires specialized simulation tools and characterization methodologies to identify logic sensitivity and the critical logic paths that dominate the product failure rate, so that correction is added only to these key components [1].

In SoC, the proportion of memory on an SoC die crossed the 50% level in 2002 and it increases to 90% of the SoC die area in 2010. Current research suggests that the average rate of failure for complex chips may be in excess of four errors per year, which can be translated into 29,000 FITs per a complex chip approximately [11].

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