

---

# Jayram, Nageswaran Moorkanikara

Email: [m.n.jayram@gmail.com](mailto:m.n.jayram@gmail.com)  
Phone: +1-949-331-4006  
Web: [www.ics.uci.edu/~jmoorkan](http://www.ics.uci.edu/~jmoorkan)

Address:  
2833 Verano Place,  
Irvine CA 92617

---

## Field(s) of interest

Brain-Inspired Computing, Computational Neuroscience, Reconfigurable and multiprocessor architectures, parallel programming on high-performance architecture, VLSI CAD for System-on-Chip (synthesis and verification), Embedded System Design

## Academic background

1. **University of California, Irvine** 2005 - 2010  
PhD Student in Computer Science (GPA: 3.97/4)  
Thesis Topic: Framework for Spike-based Neural Network Modeling on High-Performance Graphics Architectures  
Thesis Advisor: Prof. Nikil Dutt, Chancellor's Professor at UCI  
Thesis Co-advisor: Prof. Jeffrey L Krichmar, Associate Professor, Department of Cognitive Sciences
2. **Indian Institute of Technology, Delhi, India** 2000 - 2002  
Master of Technology in VLSI Design Tools and Technology (CGPA: 9.20/10.0)  
Master Thesis: Kahn process networks based application modeling for multiprocessors
3. **Government College of Technology, Coimbatore, India** 1995 - 1999  
Bachelor in Electronics and Communication Engineering, (Grade: 89/100)

## Academic/Teaching Experience

- Graduate Research Assistant, Cognitive Science Department, UC, Irvine** May '08 - present
- DARPA SYNAPSES Project: As a part of my research, I am focusing on high-performance architectures like NVIDIA GPUs and IBM CELL for simulation of brain-inspired computing algorithms specially targeting vision applications. I am working on applications and principles of spiking neural networks, which incorporates detailed temporal aspects of spike patterns for its computation. I am also involved in the development of spike-based cortical simulator that allows virtual (or real) robot to identify novel objects in the given environment.
- Teaching Assistant, University of California, Irvine** Sep '09 - Mar '10
- ICS 22: Introduction to Computer Science II, Winter 2010
  - CS 153: Logic Design Laboratory, Fall 2009
- Graduate Research Assistant, Computer Science Department, UC, Irvine** Jan '06 - April '08
- Brain-Inspired Computing Project: In this work we looked into various techniques to model the hierarchical vision processing carried out by the human brain. We also mapped these brain-inspired vision algorithms on IBM CELL processors and FPGA architectures.

## Industrial Experience

- Research Engineer, Philips Research Labs, The Netherlands** Mar '02 – May '05 (3.5 years)
- Multiprocessor SoC design and verification for Media processing applications
  - HW-SW and Mixed-HW Co-simulation framework for multiprocessor simulation
  - Implementation and optimization of H.264 decoder on Tri-Media VLIW processor
  - Application level performance metrics and implementation for multiprocessors applications
- Summer Intern, Freescale Semiconductors, Austin** July '06 – Aug '06 (3 months)
- Dynamic simulation techniques for architecture description languages for PowerPC
- Summer Intern, Broadcom Corporation, San Diego** July '07 – Sep '07 (3 months)
- Design and Simulation of ARM-Cortex based SoC for Bluetooth systems

## Selected publications/Reports

### Journal and Peer-reviewed Conference Publications

1. **J.M. Nageswaran**, N. Dutt, J.L. Krichmar, A. Nicolau, and A.V. Veidenbaum, "A Configurable Simulation Environment for the Efficient Simulation of Large-Scale Spiking Neural Networks on Graphics Processors", Neural Networks, vol. 22, Jul. 2009, pp. 791-800

2. **J.M. Nageswaran**, N. Dutt, J.L. Krichmar, A. Nicolau, and A. Veidenbaum, "Efficient simulation of large-scale spiking neural networks using CUDA graphics processors", Proceedings of the 2009 international joint conference on Neural Networks, Atlanta, Georgia, USA: IEEE Press, 2009, pp. 3201-3208
3. **J.M. Nageswaran**, Y. Wang, N. Dutt, and T. Delbrueck, "Computing Spike-based Convolution on GPUs", IEEE Intl Symposium on Circuits and Systems (ISCAS), 2009
4. **J.M. Nageswaran**, A. Felch, A. Chandrasekhar, N. Dutt, R. Granger, A. Nicolau, and A. Veidenbaum, "Brain derived vision algorithm on high performance architectures, International Journal on Parallel Programming, vol. 37, 2009, pp. 345-369.
5. A. Felch, **J.M. Nageswaran**, A. Chandrashekar, J. Furlong, N. Dutt, R. Granger, A. Nicolau, and A. Veidenbaum, "Accelerating Brain Circuit Simulations of Object Recognition with CELL Processors", International workshop on Innovative architecture for future generation high-performance processors and systems, 2007
6. J. Furlong, A. Felch, **J.M. Nageswaran**, N. Dutt, A. Nicolau, A. Veidenbaum, A. Chandrashekar, and R. Granger, "Novel brain-derived algorithms scale linearly with number of processing elements", Proceedings of ParaFPGA conference: parallel computing with FPGAs, 2007.
7. **J.M.Nageswaran**, R.Bos, "MPSoC verification using a unified random program approach, Microprocessor Test and Verification", IEEE 7th International Workshop on Microprocessor Test & Verification (MTV), 2006
8. S. Kiran, **J.M.Nageswaran**, P. Rao, and S.K. Nandy, "A complexity effective communication model for behavioral modeling of signal processing applications," Proceedings of the 40th annual Design Automation Conference, Anaheim, CA, USA: ACM, 2003, pp. 412-415.

#### **Book Chapter**

1. J. Eijndhoven, J. Hoogerbrugge, **J.M.Nageswaran**, P. Stravers, and A. Terechko, "Cache-Coherent Heterogeneous Multiprocessing as Basis for Streaming Applications," Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices, 2005, pp. 61-80.

#### **Design Contests**

1. ASP-DAC/ Intl. Conference VLSI Design 2002, "D-mark: A Tiny DSP Processor for Efficient Implementation of Digital Filter and FFT"
2. ASP-DAC/ Intl. Conference VLSI Design 2002, "A Scalable 8 x 8 Batcher-Banyan chips for ATM switch"

#### **Poster Presentations**

1. Biologically plausible homeostasis and STDP: Stability and learning patterned inputs in spiking neural networks, International Conference on Cognitive and Neural Systems, May 2010
2. Brain Circuit Simulations: Computational models and Hardware Acceleration PhD Forum, Design Automation Conference (DAC 2009)
3. High-Performance Architectures for Accelerating Brain Circuit Simulations, Center for Cognitive Sciences, University of California, Irvine
4. Scalable Parallel Implementations of a Brain Derived Vision Algorithm on IBM CELL processors, Joint Symposium on Neural Computation, 2007
5. WASABI: high-performance heterogeneous multiprocessor, ACACES: International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems, 2005
6. Scalable Process Network Based Application Modeling For Multiprocessors, Conference on High Performance Computing in Asia Pacific Region, 2002

#### **Technical Reports**

1. Application level Performance Metrics Definition and Implementation on SpaceCAKE multiprocessor, Philips Research Technical note, 2003

#### **Awards and Recognitions**

- 1) Best paper award at International Joint Conference on Neural Networks, 2009 at Atlanta Georgia
- 2) Best participant award in 2008 Telluride Neuromorphic Workshop and Summer School
- 3) IBM CELL/B.E University Challenge 2007 Grand Prize winner
- 4) Three joint patents filings in multiprocessor architectures and SoC Verification
- 5) All India Rank 3 in Graduate Aptitude Test in Engineering for ECE students among over 10000 candidates (GATE 2001)
- 6) Graduate Fellowship from Philips Semiconductors, The Netherlands for Graduate Program in VLSI Design (2001)
- 7) First rank medal for undergraduate students in Department of ECE at Government. College of Tech, INDIA(1999)

#### **Software Skills**

- Programming: C, C++, JAVA, MATLAB, Verilog, VHDL, SystemC
- Parallel programming: Nvidia CUDA, MPI, Pthreads, Programming on IBM CELL processor
- Embedded Processor Programming: TriMedia, ARM, Intel 8085/86
- EDATools: Xilinx/Altera FPGA Tools, Synopsys DC tools, Cadence Incisive tools, Magic & Tanner Layout Tools

## Open source contributions

1. Biologically realistic spiking neural network simulator on GPU  
Website: <http://www.ics.uci.edu/~jmoorkan/project/index.htm>  
Founder and lead developer of an open-source simulator that allows simulation of large-scale spiking neural networks (more than 250K neurons) on CPU and accelerated simulation on GPU
2. Brain-derived Vision model for line-object recognition  
Website: <http://sourceforge.net/projects/bdv-cell/>  
A bottom-up engine running on IBM CELL processors which allows for fast evaluation of bit-vector receptive field and used in line-based object recognition

## Academic Reviewing Services

1. Reviewer, International Journal on Parallel Programming (IJPP)
2. Reviewer, IEEE Transaction on Neural Networks (IEEE TNN)
3. Reviewer, IEEE International Conference on Circuits and Systems (ISCAS)
4. Reviewer, Transactions on HiPEAC
5. Reviewer, The IEEE Robotics and Automation Magazine (IEEE RAM)
6. Student member of IEEE, ACM and Neural Network society

## Community Services

1. Secretary and board member of SPICMACAY-UCI Chapter for promotion of Indian classical music
2. Former member of ASHA for Education, Eindhoven, an organization focusing on basic education in India

## References

- 1) To be provided on request