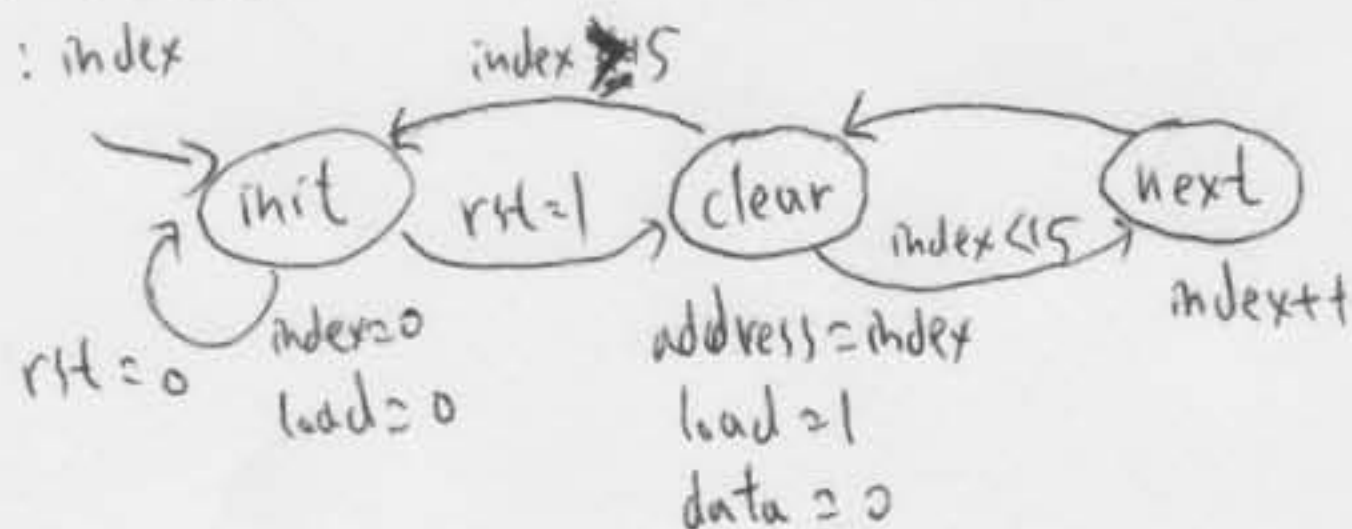


5.4

Input: rst

Outputs: address, load, data

register: index



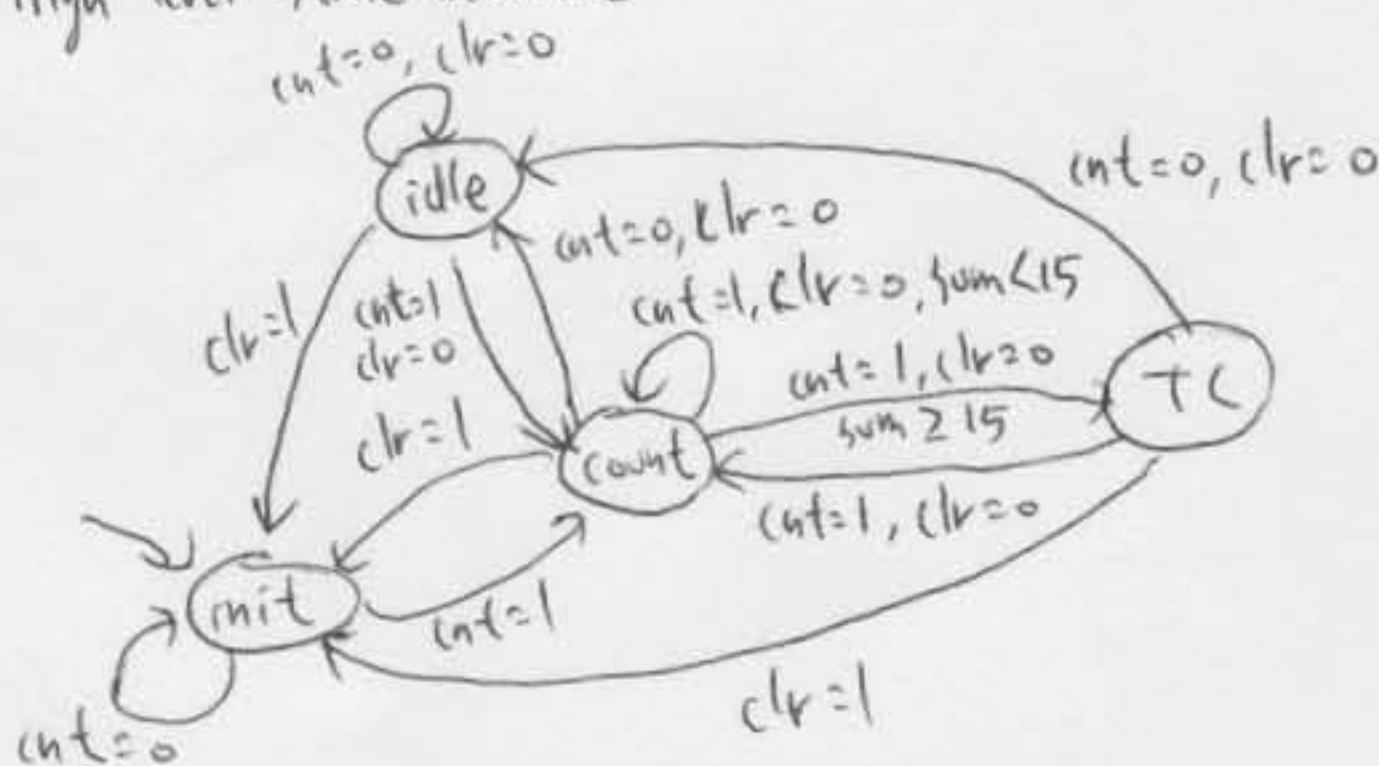
5.6

inputs: cnt, clr

outputs: tc

register: sum

High level state machine

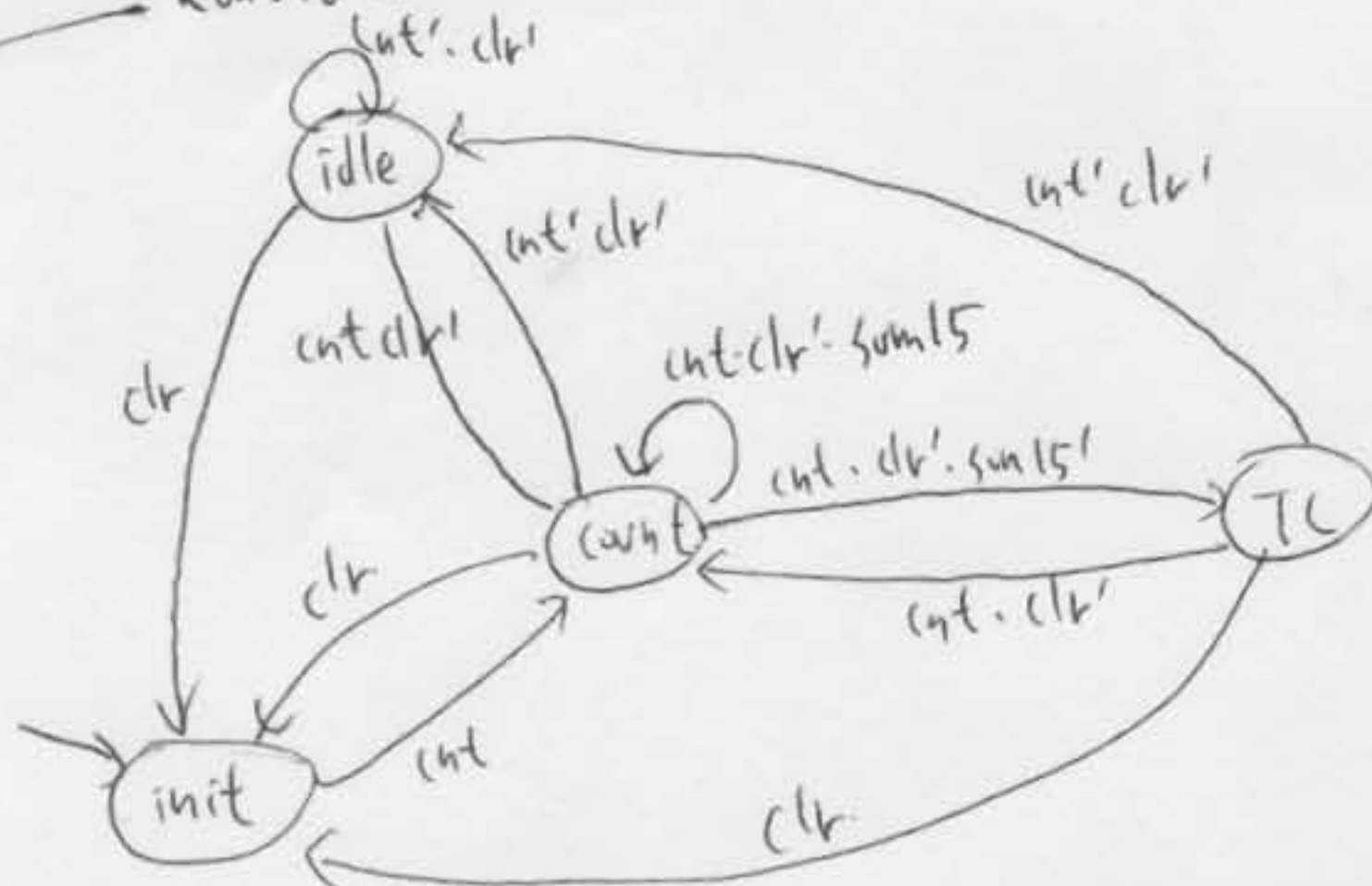


init: sum=0, tc=0

TC: sum=0, tc=1

count: sum = sum + 1

Controller FSM



~~init~~

init: clr sum = 1, tc = 0

TC: clr sum = 1, tc = 1

count: ~~clr~~ sum = 1

inputs: cnt, clr, sum=15

outputs: tc, clr sum, clr sum