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DEPARTMENT OF ELECTRONICS
INFORMATION AND BIOENGINEERING

Hardware Design and Implementation of Post-quantum Cryptographic Algorithms

The case of NTRU, HQC and CROSS

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Doctoral Programme In Information Technology

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Introduction to Post-Quantum Cryptography

NTRU: N-th degree Truncated polynomial Ring Units

HQC: Hamming Quasi-Cyclic

CROSS: Codes and Restricted Objects Signature Scheme

Concluding remarks

Introduction to Post-Quantum Cryptography

Today we assist to continuous advancements in the computational capabilities of quantum computers:

- more powerful QPUs: up to 1121 qubits (Condor, IBM)
- longer coherency time: circuits w/ 5000 gates (Heron, IBM)
- higher density: 100 nm pitch between qubits (spin qubit, Intel)

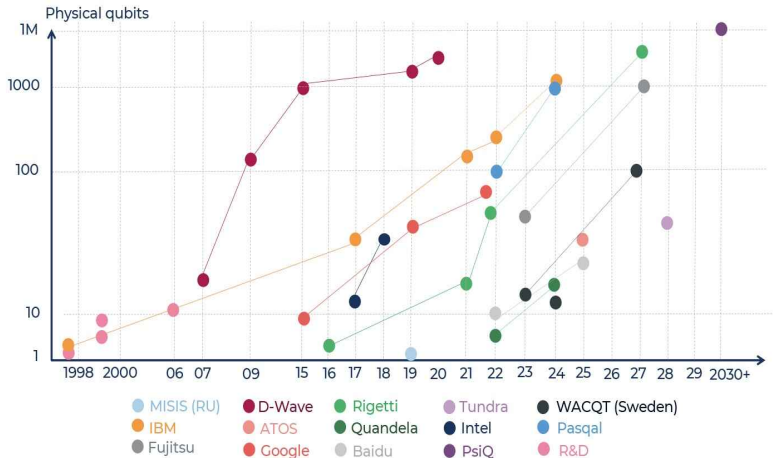
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- more powerful QPUs: up to 1121 qubits (Condor, IBM)
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There are still several limitations afflicting the current technology, such as producing a scalable quantum memory [1], but many other roadblocks have been solved in the past few years [2].

Quantum computing

Source: Quantum Technologies 2023 report, Yole Intelligence, 2023



The quantum threat

Grover's algorithm [3] for quantum computers allows to finding zeros in a function quadratically faster compared to the best classical solution for regular computers.

Shor's algorithm [4] solves the order finding problem with a superpolynomial speedup w.r.t. non-quantum algorithms.

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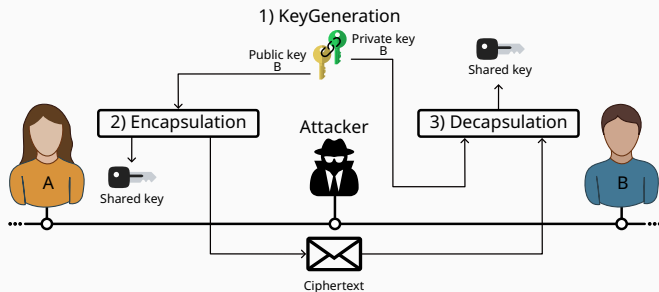
Shor's algorithm [4] solves the order finding problem with a superpolynomial speedup w.r.t. non-quantum algorithms.

The (big) trouble

All the hard problems at the base of the widely used public-key cryptosystems (e.g., ECC and RSA) are reducible to the order finding problem!

Post-Quantum Cryptography (PQC)

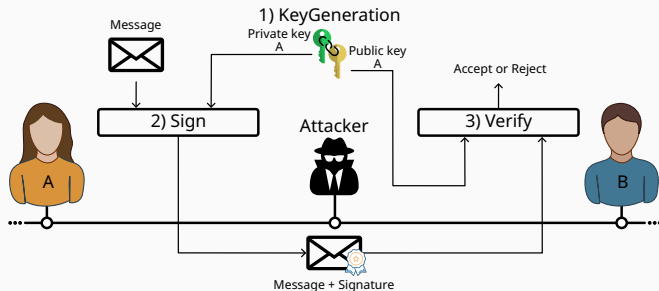
In 2016 the U.S. National Institute of Standards and Technology (NIST) started a standardization process of quantum-resistant asymmetric cryptoschemes implementing a Key Establishment Mechanism (KEM) or Digital Signature Algorithm (DSA).



Key Establishment Mechanism

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Digital Signature Algorithm

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BIG QUAKE	Gravity-SPHINCS	LUOV
BIKE	Guess Again	McNie
CFPKM	Gui	Mersenne-756839
Classic McEliece	HILA5	MQDSS
Compact LWE	HiMQ-3	NewHope
CRYSTALS-DILITHIUM	HK-17	NTRUencrypt
CRYSTALS-KYBER	HQC	NTRU-HRSS-KEM
DAGS	KCL	NTRU Prime
Ding Key Exchange	KINDI	NTS-KEM
DME	LAC	Odd Manhattan
DRS	LAKE	Ouroboros-R
DualModeMS	LEDAkem	Picnic
Edon-K	LEDApkc	Post-quantum RSA Encryption
EMBLEM/R.EMBLEM	Lepton	Post-quantum RSA Signature
FALCON	LIMA	pqNTRUSign
FrodoKEM	Lizard	pqsigRM
GeMSS	LOCKER	QC-MDPC-KEM
Giophantus	LOTUS	qTESLA
RaCoSS	Round2	SPHINCS+
Rainbow	RQC	SRTPI
Ramstake	RVB	Three Bears
RankSign	SABER	Titanium
RLCE-KEM	SIKE	WalnutDSA

Some numbers:

- 82 submissions
- 69 valid schemes
- 26 after 1st round
- 7 after 2nd round

Post-Quantum Cryptography (PQC)

In 2016 the U.S. National Institute of Standards and Technology (NIST) started a standardization process of quantum-resistant asymmetric cryptoschemes implementing a Key Establishment Mechanism (KEM) or Digital Signature Algorithm (DSA).

Many other national and international standardization bodies are also working on Post-Quantum Cryptography (PQC):

- European Telecom. Standards Institute (ETSI) [5], [6]
- French Cybersecurity Agency (ANSSI) [7]
- German Federal Office for Information Security (BSI) [8], [9]
- Chinese Association for Cryptologic Research (CACR)
- Internet Engineering Task Force (IETF)
- International Organization for Standardization (ISO)

This is the current situation after the conclusion of the first standardization contest in March 2025:

- **CRYSTALS-Kyber**: lattice-based ML-KEM, FIPS 203
- **CRYSTALS-Dilithium**: lattice-based ML-DSA, FIPS 204
- **SPHINCS⁺**: hash-based SLH-DSA, FIPS 205
- **FALCON**: lattice-based FN-DSA, WIP
- **HQC**: code-based KEM, WIP

Post-Quantum Cryptography (PQC)

Now it's time to plan the transition to PQC [10], [11].

It is generally advised to employ a hybrid scheme combining a pre- and post-quantum cryptoscheme.

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Breaking Rainbow Takes a Weekend on a Laptop

Ward Beullens^(✉) 

IBM Research, Zurich, Switzerland

`wbe@zurich.ibm.com`

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Breaking Rainbow Takes a Weekend on a Laptop

IBM

An Efficient Key Recovery Attack on SIDH

Wouter Castryck^{1,2}  and Thomas Decru¹ 

¹ imec-COSIC, KU Leuven, Leuven, Belgium
wouter.castryck@esat.kuleuven.be

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thomas.decru@esat.kuleuven.be

Post-Quantum Cryptography (PQC)

A new standardization effort seeking for an alternate digital signature algorithm not based on structured lattice is still ongoing.

<u>Code-Based</u>	<u>Lattice-Based</u>	<u>MPC-in-the-Head</u>	<u>Multivariate</u>
CROSS	EagleSign	Biscuit	3WISE
Enhanced pqsigRM	EHTv4	MIRA*	DME-Sign
FuLeeca	HAETAE	MiRitH*	HPPC
LESS	HAWK	MQOM	MAYO
MEDS	HuFu	PERK	PROV
WAVE	Raccoon	RYDE	QR-UOV
	SQUIRRELS	SDitH	SNOVA
<u>Other</u>			TUOV
ALTEQ	<u>Symmetric-Based</u>	<u>Isogeny-Based</u>	UOV
eMLE-Sig 2.0	AlMer	SQLsign	VOX
KAZ-SIGN	Ascon-Sign		
PREON	FAEST		
Xifrat1-Sign.I	SPHINCS-alpha		

Challenges in designing and implementing PQC

Designing a new cryptographic algorithm is a challenging task:

- parameter selection, producing adequate security proofs
- trying algebraic attacks for key/message recovery
- perf. evaluation in protocols in emulated/real environments
- explore optimization corners: sub-algorithms, vectorization
 - in terms of latency, area, efficiency, power consumptions
- physical security evaluation: side-channel attacks, fault attacks

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Ph.D. thesis contribution

We are focusing on the design of dedicated hardware accelerators for the full PQC algorithms NTRU, HQC, and CROSS.

NTRU: N-th degree Truncated polynomial Ring Units

The N -th degree Truncated polynomial Ring Units (NTRU) is a lattice-based KEM relying on the hardness of the Shortest Vector Problem (SVP) – and the closely related Closest Vector Problem (CVP) – in a n -dimensional integer lattice, both NP-hard problems.

The original work is dated back in 1998 [12], and several iterations improved the performance and security estimation.

In the PQC contest, there were three independent submissions:

NTRU-HPS, **NTRU-HRSS**, Streamlined NTRU Prime

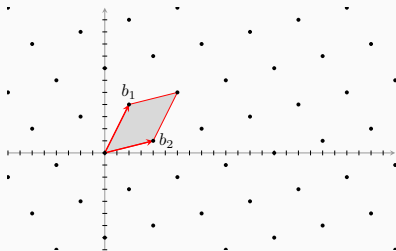
Compared to the standardized ML-KEM algorithm, NTRU can scale the security margin more easily, but has slightly large ciphertext sizes and a particularly slow key generation procedure.

Introduction to NTRU

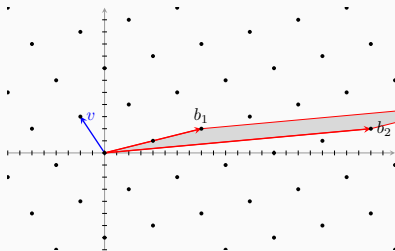
The Shortest Vector Problem

Given $k \in \mathbb{N}$ linearly independent vectors $b_i \in \mathbb{R}^n$, with $1 \leq i \leq k$ and $k \leq n$, an instance of a lattice $\mathcal{L}$ is the set of points in $\mathbb{R}^n$:

$$\mathcal{L} := \Lambda(b_1, b_2, \dots, b_k) = \left\{ \sum_{i=1}^k a_i b_i \mid a_i \in \mathbb{Z} \right\} \subseteq \mathbb{R}^n$$



$$b_1 = [4, 2], b_2 = [2, 4]$$



$$b_1 = [8, 2], b_2 = [22, 2]$$

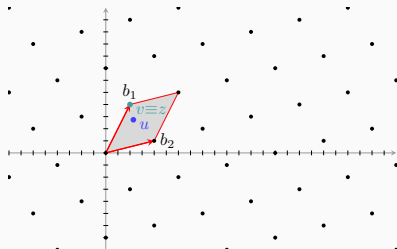
SVP in the integer lattice $\mathcal{L} \subset \mathbb{Z}^2$

Introduction to NTRU

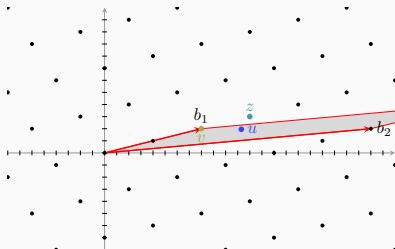
The Closest Vector Problem

Given $k \in \mathbb{N}$ linearly independent vectors $b_i \in \mathbb{R}^n$, with $1 \leq i \leq k$ and $k \leq n$, an instance of a lattice $\mathcal{L}$ is the set of points in $\mathbb{R}^n$:

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CVP in the integer lattice $\mathcal{L} \subset \mathbb{Z}^2$

NTRU makes use of arithmetic in the quotient polynomial ring

$$R = \mathbb{Z}[x] / \langle x^n - 1 \rangle \quad \text{with } (x^n - 1) = \Phi_1 \Phi_n$$

$n \in \{509, 677, 701, 821\}$ prime numbers $\Rightarrow \Phi_1, \Phi_n$ are irreducible

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$$n \in \{509, 677, 701, 821\} \text{ prime numbers} \Rightarrow \Phi_1, \Phi_n \text{ are irreducible}$$

Internally the scheme actually works with three polynomial rings:

$$R_q = \mathbb{Z}_q[x] / \langle \Phi_1 \Phi_n \rangle \quad S_q = \mathbb{Z}_q[x] / \langle \Phi_n \rangle \quad S_p = \mathbb{Z}_p[x] / \langle \Phi_n \rangle$$

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- **large** polynomial: coefficients in $\mathbb{Z}_q$, $q \in \{2048, 4096, 8192\}$
- **small** polynomial: coefficients in $\mathbb{Z}_p = \mathbb{Z}_3$
 - **fixed-weight**: $d \in \{127, 255\}$ coefficients eq. to 1 and -1
 - **variable-weight**: any number of non-null coefficients

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Further constraints to make a deterministic cryptographic scheme:

- $\gcd(p, q) = 1, p \ll q$
- $q > (6d + 1)p$

Background

Arithmetic in $R_q = \mathbb{Z}_q / \langle x^n - 1 \rangle$

$f = f_{n-1}x^{n-1} + \dots + f_1x + f_0 \in R$ seen as $[f_{n-1}, \dots, f_1, f_0] \in \mathbb{Z}^n$

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Polynomial addition

Let $a, b \in R_q$, their sum $c = a + b$ has coefficients

$$c_k \equiv_q a_k + b_k, \quad \forall k \in \{0, \dots, n-1\}$$

Background

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Polynomial product (circular convolution)

Let $a, b \in R_q$, their product $c = a \cdot b$ has coefficients

$$c_k \equiv_q \sum_{i+j \equiv k \pmod n} a_i \cdot b_j, \quad \forall k \in \{0, \dots, n-1\}$$

NTRU KEM scheme

NTRU.KEM-KeyGeneration

Require: None

Ensure: $pk = h^{p_{kd}}$

$sk = (f^{p_{kd}}, f_p^{p_{kd}}, h_q^{p_{kd}}, s \in \{0, 1\}^{256})$

- 1: $\gamma \xleftarrow{\$} \{0, 1\}^{320}$
 - 2: $(s, \text{str}_f, \text{str}_g) \leftarrow \text{CSPRNG}(\gamma, \{0, 1\}^{8 \cdot (n-1)} \times \{0, 1\}^\beta)$
 - 3: $f \leftarrow \text{CSPRNG}(\text{str}_f, \mathcal{L}_f)$, $g \leftarrow \text{CSPRNG}(\text{str}_g, \mathcal{L}_g)$ $\triangleright$ Sample two random small polys
 - 4: $f_p \leftarrow f^{-1} \bmod (p, \Phi_n)$ $\triangleright$ Inverse ring element
 - 5: $G \leftarrow p \cdot g$
 - 6: $v \leftarrow (G \cdot f) \bmod (q, \Phi_n)$ $\triangleright$ Small poly by a large poly multiplication
 - 7: $v_q \leftarrow v^{-1} \bmod (q, \Phi_n)$ $\triangleright$ Inverse ring element
 - 8: $h \leftarrow (v_q \cdot G \cdot G) \bmod (q, \Phi_1 \Phi_n)$ $\triangleright$ Two small poly by a large poly multiplications
 - 9: $h_q \leftarrow (v_q \cdot f \cdot f) \bmod (q, \Phi_1 \Phi_n)$ $\triangleright$ Two small poly by a large poly multiplications
 - 10: $h^{p_{kd}} \leftarrow \text{Pack}_q(h)$; $f^{p_{kd}} \leftarrow \text{Pack}_p(f)$; $f_p^{p_{kd}} \leftarrow \text{Pack}_p(f_p)$; $h_q^{p_{kd}} \leftarrow \text{Pack}_q(h_q)$
 - 11: **return** $pk = h^{p_{kd}}$, $sk = (f^{p_{kd}}, f_p^{p_{kd}}, h_q^{p_{kd}}, s)$
-

Lattice	Polynomials	HPS	HRSS
$\mathcal{L}_f$	f	variable-weight	variable-weight ⁺
$\mathcal{L}_g$	g	fixed-weight (d)	variable-weight ⁺

NTRU KEM scheme

NTRU.KEM-Encapsulation

Require: $pk = h^{pkd}$

Ensure: $ctx = c^{pkd}$

$K \in \{0, 1\}^{256}$

1: $h \leftarrow \text{Unpack}_q(h^{pkd})$

2: $\gamma \xleftarrow{\$} \{0, 1\}^{320}$

3: $(\text{str}_r, \text{str}_m) \leftarrow \text{CSPRNG}(\gamma, \{0, 1\}^{8 \cdot (n-1)} \times \{0, 1\}^\beta)$

4: $r \leftarrow \text{CSPRNG}(\text{str}_r, \mathcal{L}_r); \quad m \leftarrow \text{CSPRNG}(\text{str}_m, \mathcal{L}_m) \triangleright \text{Sample two random small polys}$

5: $m' \leftarrow \text{Lift}(m) \quad \triangleright \text{Map Lift : } S_p \mapsto R_q \text{ s.t. } \text{Lift}(m) \bmod (p, \Phi_n) = m$

6: $c \leftarrow (r \cdot h + m') \bmod (q, \Phi_1 \Phi_n) \quad \triangleright \text{Small poly by a large poly multiplication}$

7: $c^{pkd} \leftarrow \text{Pack}_q(c); \quad r^{pkd} \leftarrow \text{Pack}_p(r); \quad m^{pkd} \leftarrow \text{Pack}_p(m)$

8: $K \leftarrow \text{Hash}(r^{pkd} || m^{pkd})$

9: **return** c^{pkd}, K

Lattice	Polynomials	HPS	HRSS
L_r	r	variable-weight	variable-weight
L_m	m	fixed-weight (d)	variable-weight
$\text{Lift}(\cdot)$		sign extension	$\Phi_1 \cdot ((a/\Phi_1) \bmod (p, \Phi_n))$

NTRU KEM scheme

NTRU.KEM-Decapsulation

Require: $sk = (f_p^{\text{pkd}}, f_p^{\text{pkd}}, h_q^{\text{pkd}}, s)$

$ctx = c^{\text{pkd}}$

Ensure: $K \in \{0, 1\}^{256}$

- 1: $f \leftarrow \text{Unpack}_q(f_p^{\text{pkd}}); f_p \leftarrow \text{Unpack}_q(f_p^{\text{pkd}}); h_q \leftarrow \text{Unpack}_q(h_q^{\text{pkd}}); c \leftarrow \text{Unpack}_q(c^{\text{pkd}})$
 - 2: $\triangleright a = (r \cdot h + m) \cdot f = (r \cdot p \cdot f_p \cdot g + m) \cdot f = r \cdot p \cdot g + f \cdot m \quad \triangleleft$
 - 3: $a \leftarrow (c \cdot f) \bmod (q, \Phi_1 \Phi_n) \quad \triangleright \text{Small poly by a large poly multiplication}$
 - 4: $m \leftarrow (a \cdot f_p) \bmod (p, \Phi_n) \quad \triangleright \text{Small poly by a large poly multiplication}$
 - 5: $m' \leftarrow \text{Lift}(m) \quad \triangleright \text{Map Lift : } S_p \mapsto R_q \text{ s.t. } \text{Lift}(m) \bmod (p, \Phi_n) = m$
 - 6: $r \leftarrow ((c - m') \cdot h_q) \bmod (q, \Phi_n) \quad \triangleright \text{Large poly by a large poly multiplication}$
 - 7: $r^{\text{pkd}} \leftarrow \text{Pack}_p(r); m^{\text{pkd}} \leftarrow \text{Pack}_p(m)$
 - 8: $K_1 \leftarrow \text{Hash}(r^{\text{pkd}} \| m^{\text{pkd}}); K_2 \leftarrow \text{Hash}(s \| c^{\text{pkd}})$
 - 9: **if** $(r, m) \notin \mathcal{L}_r \times \mathcal{L}_m \vee c \not\equiv 0 \bmod (q, \Phi_1)$ **then** $K = K_2$ **else** $K = K_1$
 - 10: **return** K
-

line 3: since $a \in R_q$, no actual mod q is performed

line 4: performing mod p removes the first term containing the randomness r , obtaining $f \cdot f_p \cdot m$

Multiplication in $R_q = \mathbb{Z}_q / \langle x^n - 1 \rangle$ – Comba algorithm

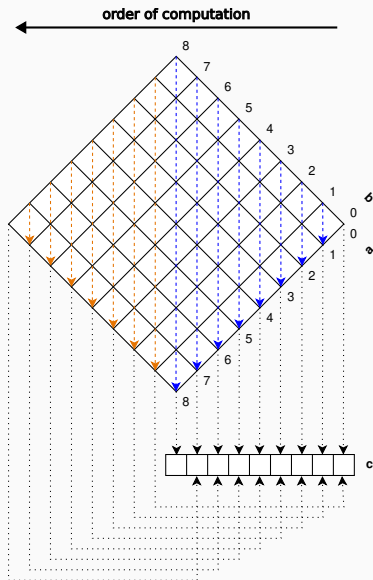
Comba multiplication

Require: $a \in R_q, b \in R_q$

Ensure: $c \in R_q \mid c = a \cdot b$

```
1:  $c \leftarrow 0$ 
2: for  $j \leftarrow 0$  to  $n-1$  do
3:   for  $i \leftarrow 0$  to  $j$  do
4:      $t \leftarrow t + a_{j-i} \cdot b_i$ 
5:    $c_j \leftarrow c_j + t$   $\triangleright$  To memory
6: for  $j \leftarrow 0$  to  $n-2$  do
7:   for  $i \leftarrow 0$  to  $j$  do
8:      $t \leftarrow t + a_{n-1-j+i} \cdot b_{n-1-i}$ 
9:    $c_{n-1-j} \leftarrow c_{n-1-j} + t$   $\triangleright$  To memory
10: return  $c$ 
```

Employs a single scalar multiplier and an adder.



Multiplication in $R_q = \mathbb{Z}_q / \langle x^n - 1 \rangle$ – x-net algorithm

a and c are stored in flip-flops. One coefficient of b processed per CC by n multiply-and-accumulate units (MACs).

x-net multiplication

Require: $a \in R_q, b \in R_q$

Ensure: $c \in R_q \mid c = a \cdot b$

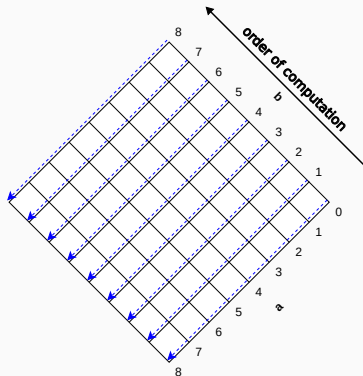
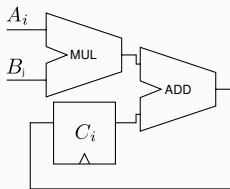
1: $c \leftarrow 0$

2: **for** $j \leftarrow 0$ **to** $n - 1$ **do**

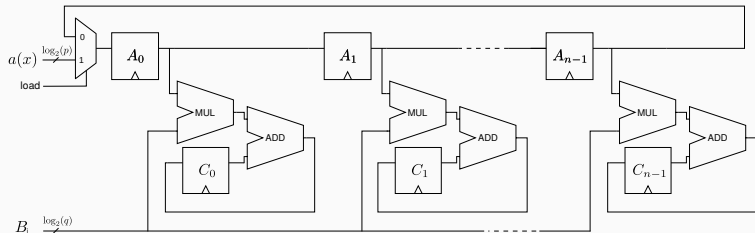
3: $c \leftarrow c + b_j \cdot a$ $\triangleright n$ parallel MACs

4: $a \leftarrow a \cdot [0, 1, 0, \dots, 0] \bmod x^n - 1$ $\triangleright$ Rotation

5: **return** c



Multiplication in $R_q = \mathbb{Z}_q / \langle x^n - 1 \rangle$ – x-net algorithm



Poly multiplication with n coefficients performed in n CC.

If $a \in S_p$:

- scalar multiplications replaced with a 3-input multiplexer
- three scalar mul. results computed only once and distributed

Lift $S_p \mapsto R_q$

Lift operation in NTRU-HRSS [13] – $\Phi_1 \cdot ((a/\Phi_1) \bmod (p, \Phi_n))$ without multiplications

Require: $a \in S_p$

Ensure: $b \in \mathcal{R}_q \mid (b) \bmod (p, \Phi_n) = a$

```
1: for  $i \leftarrow 0$  to  $n - 2$  do
2:    $c_i \leftarrow (1 - i) \bmod p$                                  $\triangleright c \leftarrow (1/\Phi_1) \bmod (p, \Phi_n)$  for NTRU parameters
3: for  $i \leftarrow 0$  to  $p - 1$  do
4:    $d_i \leftarrow \langle x^i \bar{c}, a \rangle$                                  $\triangleright$  inner-product of  $a$  with the rotated reversal map of  $c$ 
5: for  $i \leftarrow p$  to  $n - 1$  do
6:    $d_i \leftarrow d_{i-p} - \sum_{j=0}^{p-1} a_{i-j}$ 
7:  $d_0 \leftarrow d_0 - d_{n-1} \bmod p$ 
8:  $b_0 \leftarrow -d_0$ 
9:  $\triangleright$  multiplication by  $\Phi_1$  replaced by additions  $\triangleleft$ 
10: for  $i \leftarrow 1$  to  $n - 1$  do
11:    $d_i \leftarrow d_i - d_{n-1} \bmod p$ 
12:    $b_i \leftarrow d_{i-1} - d_i \bmod q$ 
13: return  $b$ 
```

2 poly multiplications as $8n$ scalar additions/subtractions

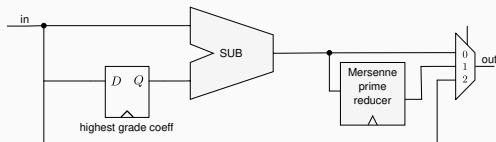
Embedding $E_1 : R_q \mapsto S_q$ and $E_2 : R_q \mapsto S_p$

Moving from ring R to S is efficiently performed subtracting the coefficient with highest grade x^{n-1} to all the others.

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Moving from ring R to S is efficiently performed subtracting the coefficient with highest grade x^{n-1} to all the others.

If $S = S_p$ the coefficient-wise reductions modulo p are computed with a pipelined Mersenne prime reduction algorithm (only adds).



Multiple coefficients can be processed in parallel.

Variable-weight small polynomials

Two strategy for sampling each small ternary coefficients:

- reduce an 8-bit number $\bmod p$ via Mersenne prime algorithm: constant execution time, approximated uniform distribution
- rejection of the single invalid encoding of a random 2-bit string: fewer bits from PRNG, perfect uniform distribution

In both cases, the parallel computation of more than one coefficient is limited only by the pressure onto the PRNG.

Sample random polynomial in $\mathcal{S}_p$

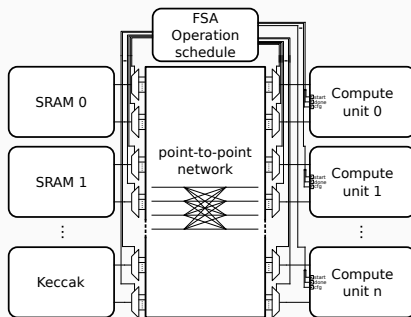
Fixed-weight small polynomials

Generate a polynomial with the first d coefficients set as 1, and the following d coefficients set as -1, then scramble it

When caches are not in use, the Fisher-Yates shuffle algorithm is safe to use as memory has a constant time access.

Operations schedule

Top-Level Design configuration

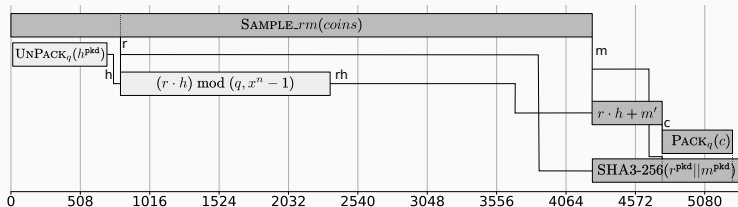


Top-Level Design (TLD) configuration implementing a KEM primitive.

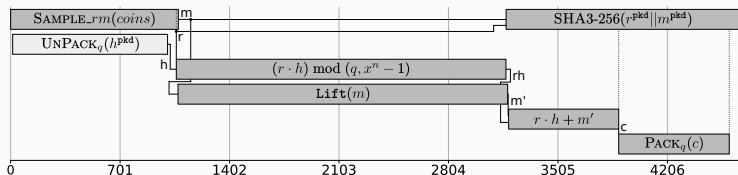
We employed four Simple Dual-Port memories, which are connected in every moment to a specific compute unit (e.g., polynomial multiplier) by global Finite State Automata (FSA) following a fixed schedule of operations.

Operations schedule

Schedule for NTRU.KEM-Encapsulation



NTRU-HPS ($q = 2048, n = 509$)

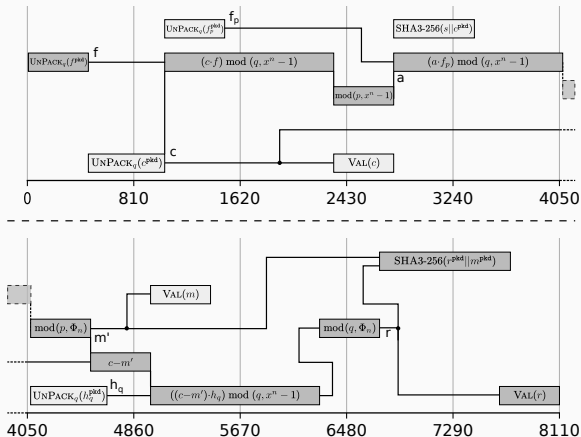


NTRU-HRSS ($q = 8192, n = 701$)

Schedule of the NTRU.KEM-Encapsulation with a x-net multiplier.
The x axis represents the latency (number of clock cycles).

Operations schedule

Schedule for NTRU.KEM-Decapsulation



NTRU-HPS ($q = 2048, n = 509$)

Schedule of the NTRU.KEM-Decapsulation (HPS variant) with a x -net multiplier. The HRSS variant includes also the Lift operation. The x axis represents the latency (number of clock cycles).

Experimental results

Design Space Exploration on FPGA

We synthesized the KEM-Encapsulation and KEM-Decapsulation in separate top-level modules on a AMD ZYNQ UltraScale+ FPGA.

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The fully decoupled arithmetic components allowed us to conduct a Design Space Exploration (DSE) considering:

- all the four parameter sets defined by **HPS** and **HRSS** variants
- either **x-net** and **Comba** polynomial multiplier algorithms
- variable-weight sampler based either on **rejection** or **modulo** algorithms
- varying the degree of computing parallelism per arithmetic component

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- varying the degree of computing parallelism per arithmetic component

The solutions with lowest latency and Area-Time product (highest efficiency) were compared with the State of the Art.

Experimental results

Comparison with the state-of-the-art

NTRU.KEM-Encapsulation						
Sec. lvl.	NTRU Variant	Work	Freq.	Area eSlice	Latency μ s	AT prod.
1	hps2048509	This work	400	6647	10.9	72.4
3	hps2048677	This work [14]	400	7968	14.8	117
			250	7642	14.8	113
	hrss701	This work [14]	400	9007	7.2	64.8
			300	8404	7.4	62.1
5	sntrup761	[15]	289	9760	17.3	168
			289	9760	17.3	168
5	hps4096821	This work [14]	400	9318	17.9	166
			250	9591	18.3	175

NTRU.KEM-Decapsulation						
Sec. lvl.	NTRU Variant	Work	Freq.	Area eSlice	Latency μ s	AT prod.
1	hps2048509	This work	350	74640	13.3	992
3	hps2048677	This work [14]	350	98251	17.6	1729
			300	14067	25.1	353
	hrss701	This work [14]	350	102504	21.7	2224
			300	16008	29.4	470
5	sntrup761	[15]	285	10028	38.6	387
			285	10028	38.6	387
5	hps4096821	This work [14]	350	118965	21.4	2545
			300	16243	34.0	552

Experimental results

ASIC synthesis

Synthesis using a 40 nm tech library and slow process corner 1.15V@40°C

NTRU.KEM-Encapsulation													
Mul. type	NTRU Variant	Area ($10^3 \mu\text{m}^2$)									Latency		
		add	sample	Keccak	q pack	k gen	$\mathcal{R}_p \times \mathcal{R}_q$	q unp.	lift	Total	Freq.	μs	
x-net	hps2048509	0.66	2.76	39.12	1.12	2.64	90.40	1.41	-	140.19	700	6.2	
	hps2048677	0.68	2.97	39.16	1.11	2.67	120.44	1.41	-	170.44	700	8.4	
	hps4096821	0.73	2.95	39.28	0.82	2.68	161.21	1.07	-	211.05	700	10.2	
	hrss701	0.83	1.36	40.24	1.26	2.67	148.91	1.54	1.87	201.15	700	4.1	
Comba	hps2048509	0.39	2.92	41.56	1.14	1.63	1.22	1.39	-	51.52	750	349.2	
	hps2048677	0.42	3.01	40.06	1.13	1.65	1.30	1.40	-	50.30	750	616.1	
	hps4096821	0.44	3.00	40.29	0.82	1.67	1.31	1.07	-	49.91	750	904.7	
	hrss701	0.47	2.40	40.96	1.35	1.68	1.36	1.52	1.22	52.43	750	660.4	
NTRU.KEM-Decapsulation													
Mul. type	NTRU Variant	Area ($10^3 \mu\text{m}^2$)									Latency		
		add	Keccak	k_1 gen.	k_2 gen.	$\mathcal{R}_q \times \mathcal{R}_q$ mult.	unpack p q	validat.	lift	Total	Freq.	μs	
x-net	hps2048509	0.78	40.60	0.68	2.67	268.95	1.02 1.54	0.21	-	320.06	650	7.1	
	hps2048677	0.81	40.10	0.72	2.70	359.13	1.06 1.52	0.26	-	410.03	650	9.4	
	hps4096821	0.81	38.96	0.71	2.66	495.69	1.07 1.17	0.28	-	517.80	650	11.5	
	hrss701	0.91	40.71	0.72	2.71	507.23	1.05 1.66	0.25	1.72	561.02	650	11.7	
Comba	hps2048509	0.42	41.46	0.67	1.64	1.59	1.08 1.51	0.31	-	51.45	750	1047.1	
	hps2048677	0.45	40.70	0.71	1.68	2.38	1.05 1.48	0.29	-	50.74	750	1847.6	
	hps4096821	0.46	40.14	0.72	1.68	2.49	1.07 1.17	0.30	-	50.08	750	2713.5	
	hrss701	0.50	40.33	0.71	1.69	2.66	1.09 1.63	0.31	1.14	52.26	750	1983.4	

HQC: Hamming Quasi-Cyclic

Hamming Quasi-Cyclic (HQC) is a KEM scheme which is relying on the hardness of the syndrome decoding problem on a double circulant quasi-cyclic random code.

HQC doesn't need an efficient decoder for the quasi-cyclic code, hence there's no need to obfuscate a known good code.

This is not the case for BIKE and Classic McEliece, the other two code-based PQC schemes in the final round of the PQC contest.

NIST announced that will standardize HQC as an general-purpose KEM algorithm as an alternative to ML-KEM (CRYSTALS-Kyber). In comparison to ML-KEM, HQC produces larger ciphertexts and is slightly slower, but is backed by a different hard problem.

Introduction to HQC

The 2-Quasi Cyclic Syndrome Decoding Problem

The Syndrome Decoding Problem – search variant

- $H \in \mathbb{F}_q^{(n-k) \times n}$ of a q -ary $[n, k, d]$ public random linear code
- $e \in \mathbb{F}_q^n$ the secret error vector having Hamming weight $< w$
- $s = eH^\top \in \mathbb{F}_q^{n-k}$ the syndrome associated to the error e

Given $pk = (H, s)$, find a vector $e \in \mathbb{F}_q^n$ such that $s = eH^\top$.

If the weight w of the error e is low enough, there is a single solution which is hard to find.

The double circulant quasi-cyclic variant employs a parity-check matrix composed by two matrices defined just by their first row. The other rows are a cyclic rotation of the previous ones.

The community believes that this variant retains the hardness. Currently the best attacks are the same for the generic codes.

Algebraic structure: binary polynomial ring

- R : polynomial ring $\mathbb{F}_2[x]/\langle x^p - 1 \rangle$, where p is a prime number

$a = a_0 + a_1x + \dots + a_{p-1}x^{p-1} \in R$ stored as vector $a = [a_0, a_1, \dots, a_{p-1}]$

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Moderate Density Parity Check code $\implies w \approx \sqrt{p}$

$a \in R_w$ is represented as a vector of indexes of non-zero coeffs.

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polynomial addition (+)

Coefficient-wise addition: XOR ($\oplus$) boolean operator

$$\begin{array}{rcccccc} a = & a_0 & + & a_1x & + \dots + & a_{p-1}x^{p-1} \\ b = & b_0 & + & b_1x & + \dots + & b_{p-1}x^{p-1} \\ \hline a + b = & (a_0 \oplus b_0) & + & (a_1 \oplus b_1)x & + \dots + & (a_{p-1} \oplus b_{p-1})x^{p-1} \end{array}$$
$$[a_0 \oplus b_0, a_1 \oplus b_1, \dots, a_{p-1} \oplus b_{p-1}]$$

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polynomial subtraction ($-$)

Coefficient-wise subtraction: XOR ($\oplus$) boolean operator

$$\begin{array}{rcllcl} a = & a_0 & + & a_1x & + \dots + & a_{p-1}x^{p-1} \\ b = & b_0 & + & b_1x & + \dots + & b_{p-1}x^{p-1} \\ \hline a - b = & (a_0 \oplus b_0) & + & (a_1 \oplus b_1)x & + \dots + & (a_{p-1} \oplus b_{p-1})x^{p-1} \end{array}$$
$$[a_0 \oplus b_0, a_1 \oplus b_1, \dots, a_{p-1} \oplus b_{p-1}]$$

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polynomial multiplication ($\cdot$)

Cyclic convolution: $c_i = \bigoplus_{j+k \equiv i \pmod p} a_j \otimes b_k$, $i, j, k \in \{0, \dots, p-1\}$

$$\begin{array}{rcll} a = & \textcolor{red}{a}_0 & + & a_1x + \dots + a_{p-1}x^{p-1} \\ b = & \textcolor{blue}{b}_0 & + & \textcolor{blue}{b}_1x + \dots + \textcolor{blue}{b}_{p-1}x^{p-1} \\ \hline \text{acc.} = & (\textcolor{red}{a}_0 \oplus \textcolor{blue}{b}_0) & + & (\textcolor{red}{a}_0 \oplus \textcolor{blue}{b}_1)x + \dots + (\textcolor{red}{a}_0 \oplus \textcolor{blue}{b}_{p-1})x^{p-1} \end{array}$$

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if $a \in R_w$, $b \in R$, asymptotic complexity $\Theta(pw) = \Theta(p\sqrt{p}) = \Theta(p^{1.5})$

Error correction code

- quasi-cyclic random $[2p, p, d]$ code with a public parity-check matrix $H = [I_p \mid \text{rot}(h)]$

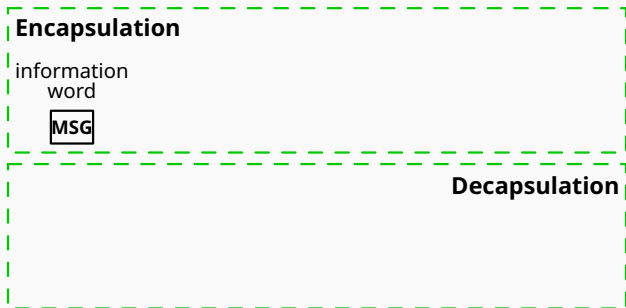
$$H = \left[\begin{array}{ccccc} 1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \end{array} \middle| \begin{array}{ccccc} h_0 & h_{p-1} & h_{p-2} & \cdots & h_1 \\ h_1 & h_0 & h_{p-1} & \cdots & h_2 \\ h_2 & h_1 & h_0 & \cdots & h_3 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ h_{p-1} & h_{p-2} & h_{p-3} & \cdots & h_0 \end{array} \right]$$

h is a random vector generated from the public key seed

Background

Error correction code(s)

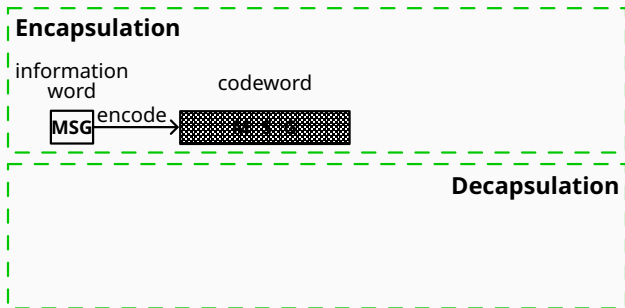
- quasi-cyclic random $[2p, p, d]$ code with a public parity-check matrix $H = [I_p \mid \text{rot}(h)]$
- public $[n_e n_i \approx p, k_e k_i, d_e d_i]$ fixed code generated by a shortened Reed-Solomon (RS) $[n_e, k_e, d_e]$ external code with a duplicated Reed-Muller (RM) $[n_i, k_i, d_i]$ internal code.



Background

Error correction code(s)

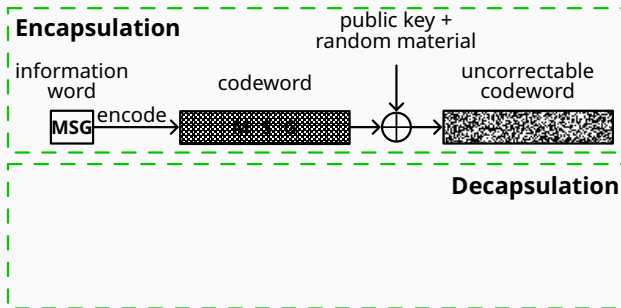
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Background

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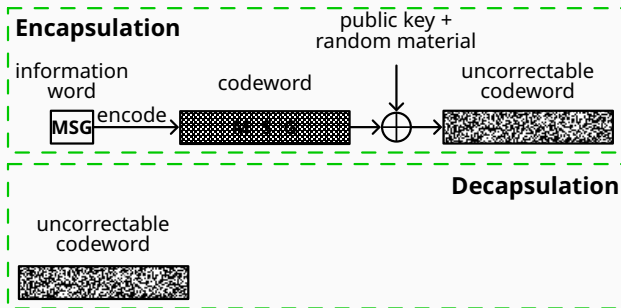
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Background

Error correction code(s)

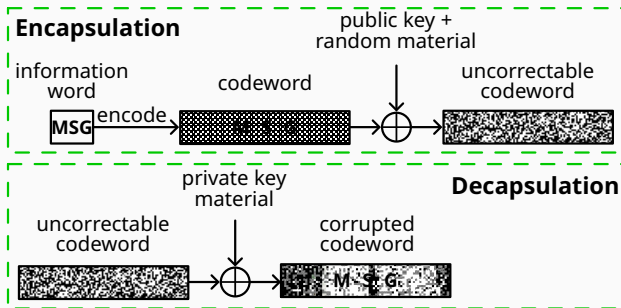
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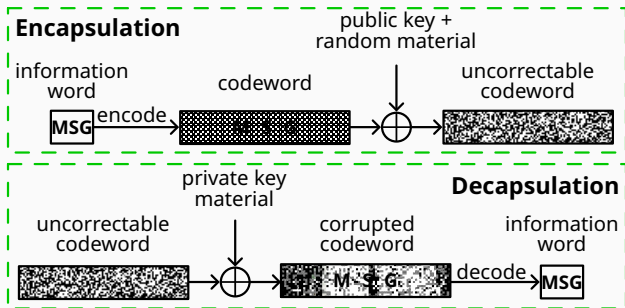
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HQC KEM scheme

HQC.KEM-KeyGeneration

Require: None

Ensure: $\text{pk} = (\varphi \in \{0, 1\}^{320}, s \in \mathbb{R})$
 $\text{sk} = (\gamma \in \{0, 1\}^{320}, \sigma \in \{0, 1\}^k, \varphi \in \{0, 1\}^{320}, s \in \mathbb{R})$

- 1: $\sigma \xleftarrow{\$} \{0, 1\}^k$
 - 2: $(\gamma, \varphi) \xleftarrow{\$} \{0, 1\}^{320} \times \{0, 1\}^{320}$
 - 3: $h \leftarrow \text{CSPRNG}(\varphi, R)$ $\triangleright$ Sample a random dense poly
 - 4: $(x, y) \leftarrow \text{CSPRNG}(\gamma, R_w \times R_w)$ $\triangleright$ Sample two random sparse polys
 - 5: $s \leftarrow x + h \cdot y$ $\triangleright$ Sparse poly by a dense poly multiplication
 - 6: **return** $\text{pk} = (\varphi, s), \text{sk} = (\gamma, \sigma, \varphi, s)$
-

HQC KEM scheme

HQC.KEM-Encapsulation

Require: $pk=(\varphi \in \{0,1\}^{320}, s \in R)$

Ensure: $ctx=(u \in R, v \in \mathbb{F}_2^{n_e n_i}, salt \in \{0,1\}^{128}), K \in \{0,1\}^{512}$

1: $m \xleftarrow{\$} \{0,1\}^k, salt \xleftarrow{\$} \{0,1\}^{128}$

2: $\theta \leftarrow \text{Hash}_G(m || \varphi || s || salt)$

3: $(e, r_a, r_b) \leftarrow \text{CSPRNG}(\theta, R_{w_e} \times R_{w_r} \times R_{w_r})$ $\triangleright$ Sample three random sparse polys

4: $h \leftarrow \text{CSPRNG}(\varphi, R)$ $\triangleright$ Sample a random dense poly

5: $u \leftarrow r_a + h \cdot r_b$ $\triangleright$ Sparse poly by a dense poly multiplication

6: $v \leftarrow \text{Encode}_G(m) + \text{Tr}(s \cdot r_b + e)$ $\triangleright$ RMRS encoding, sparse poly by a dense poly mul

7: $K \leftarrow \text{Hash}_K(m || u || v)$

8: **return** $ctx = (u, v, salt), K$

HQC KEM scheme

HQC.KEM-Decapsulation

Require: $\text{ctx} = (u \in \mathbb{R}, v \in \mathbb{F}_2^{n_e n_i}, \text{salt} \in \{0, 1\}^{128})$

$\text{sk} = (\gamma \in \{0, 1\}^{320}, \sigma \in \{0, 1\}^k, \varphi \in \{0, 1\}^{320}, s \in \mathbb{R})$

Ensure: $K \in \{0, 1\}^{512}$

- 1: $(x, y) \leftarrow \text{CSPRNG}(\gamma, R_w \times R_w)$ $\triangleright$ Sample two random sparse polys
 - 2: $m' \leftarrow \text{Decode}_G(\text{Tr}([v \| 0^{p-n_e n_i}] - u \cdot y))$ $\triangleright$ RMRS decoding, sparse poly by a dense poly mul
 - 3: $\theta' \leftarrow \text{Hash}_G(m' \| \varphi \| s \| \text{salt})$
 - 4: $(e, r_a, r_b) \leftarrow \text{CSPRNG}(\theta, R_{w_e} \times R_{w_r} \times R_{w_r})$ $\triangleright$ Sample three random sparse polys
 - 5: $h \leftarrow \text{CSPRNG}(\varphi, \mathbb{R})$ $\triangleright$ Sample a random dense poly
 - 6: $u \leftarrow r_a + h \cdot r_b$ $\triangleright$ Sparse poly by a dense poly multiplication
 - 7: $v \leftarrow \text{Encode}_G(m) + \text{Tr}(s \cdot r_b + e)$ $\triangleright$ RMRS encoding, sparse poly by a dense poly mul
 - 8: **if** $(\text{ctx} \neq \text{ctx}')$ $K' \leftarrow \text{Hash}_K(\sigma \| u \| v)$ **else** $K' \leftarrow \text{Hash}_K(m' \| u \| v)$
 - 9: **return** K'
-

Polynomial adder

Addition/subtraction $R \times R \mapsto R$

In case both operands are in R :

operand1

operand2

result

Polynomial adder

Addition/subtraction $R \times R \mapsto R$

In case both operands are in R :

- access data in blocks of $B = 128$ bits

											operand1
0	1	2	3	4	5	6	7	8	9	10	11

											operand2
0	1	2	3	4	5	6	7	8	9	10	11

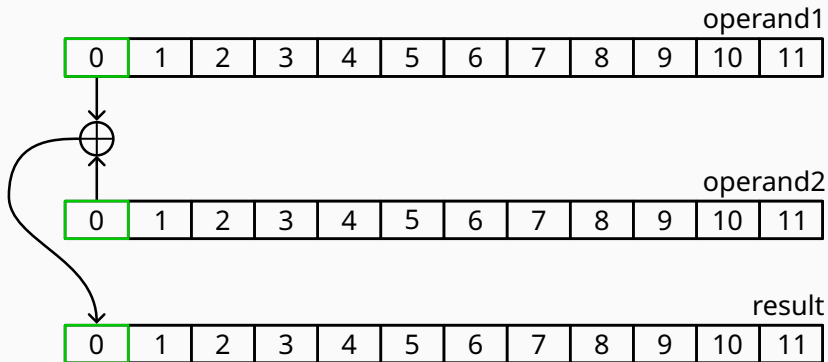
											result
0	1	2	3	4	5	6	7	8	9	10	11

Polynomial adder

Addition/subtraction $R \times R \mapsto R$

In case both operands are in R :

- access data in blocks of $B = 128$ bits
- perform the XOR operation block-wise

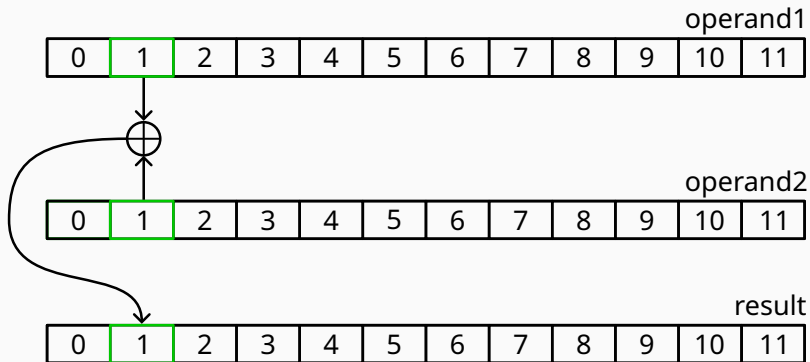


Polynomial adder

Addition/subtraction $R \times R \mapsto R$

In case both operands are in R :

- access data in blocks of $B = 128$ bits
- perform the XOR operation block-wise



Polynomial adder

Addition $R_w \times R \mapsto R$

In case operand1 in R_w and operand2 is in R :
For each index i in the vector of operand1:

operand1

544	284	302	1402	239	819	265	1053
-----	-----	-----	------	-----	-----	-----	------

operand2/result

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

Polynomial adder

Addition $R_w \times R \mapsto R$

In case operand1 in R_w and operand2 is in R :

For each index i in the vector of operand1:

- determine the operand2 block index as $\lfloor i/B \rfloor$

operand1

544	284	302	1402	239	819	265	1053
-----	-----	-----	------	-----	-----	-----	------

operand2/result

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

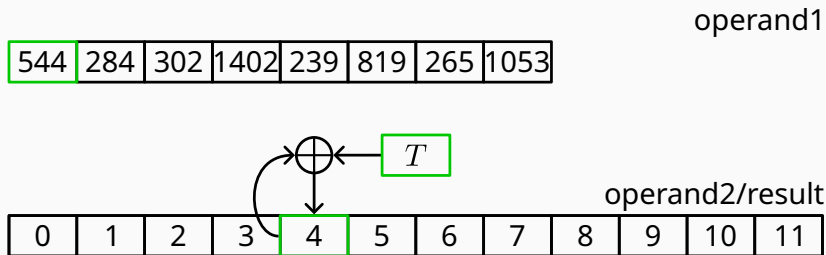
Polynomial adder

Addition $R_w \times R \mapsto R$

In case operand1 in R_w and operand2 is in R :

For each index i in the vector of operand1:

- determine the operand2 block index as $\lfloor i/B \rfloor$
- flip a single bit of that block by generating $T = 1 \ll (i \bmod B)$



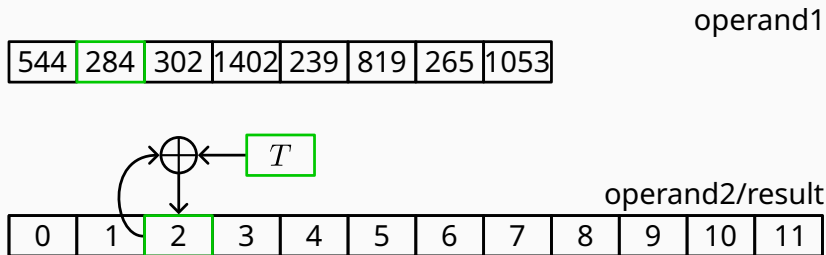
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Polynomial adder

Addition $R_w \times R \mapsto R$

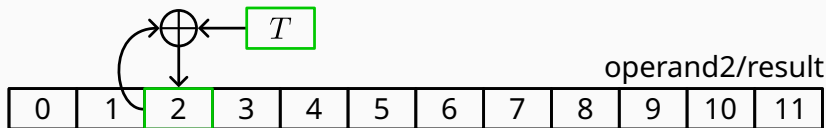
In case operand1 in R_w and operand2 is in R :

For each index i in the vector of operand1:

- determine the operand2 block index as $\lfloor i/B \rfloor$
- flip a single bit of that block by generating $T = 1 \ll (i \bmod B)$
- cannot be easily pipelined due to read-after-write dependency!

operand1

544	284	302	1402	239	819	265	1053
-----	-----	-----	------	-----	-----	-----	------



- One operand is always in R_w
- The low weight of polynomial ($\approx \sqrt{p}$) makes the schoolbook shift-and-add approach interesting: $\Theta(p^{1.5})$ asymptotic complexity

- One operand is always in R_w
- The low weight of polynomial ($\approx \sqrt{p}$) makes the schoolbook shift-and-add approach interesting: $\Theta(p^{1.5})$ asymptotic complexity
- There are faster algorithms based on the NTT with better asymptotic complexity, but:
 - the polynomial ring is not compatible with any NTT algorithm
 - memory access pattern is challenging to optimize

Polynomial multiplier: $R \times R_w$

Single index processed

$$\text{start block} = \lfloor (p - i) / B \rfloor$$

$$\text{shift amount} = \lfloor (p - i) \bmod B \rfloor$$

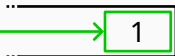
operand1

1332	862	302	1402	239	819	265	1053
------	-----	-----	------	-----	-----	-----	------

operand2

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

barrel shifter



accumulator



Polynomial multiplier: $R \times R_w$

Single index processed

$$\text{start block} = \lfloor (p - i) / B \rfloor$$

$$\text{shift amount} = \lfloor (p - i) \bmod B \rfloor$$

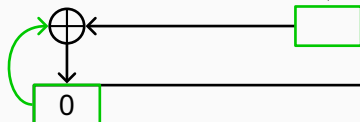
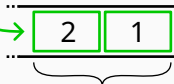
operand1

1332	862	302	1402	239	819	265	1053
------	-----	-----	------	-----	-----	-----	------

operand2

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

barrel shifter



accumulator

Polynomial multiplier: $R \times R_w$

Single index processed

$$\text{start block} = \lfloor (p - i) / B \rfloor$$

$$\text{shift amount} = \lfloor (p - i) \bmod B \rfloor$$

operand1

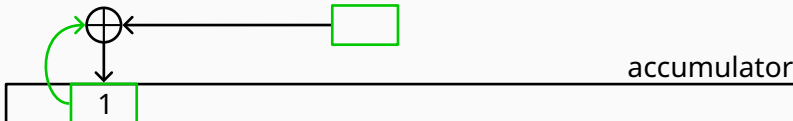
1332	862	302	1402	239	819	265	1053
------	-----	-----	------	-----	-----	-----	------

operand2

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

barrel shifter

3 2



Polynomial multiplier: $R \times R_w$
Single index processed

$$\text{start block} = \lfloor (p - i)/B \rfloor$$

$$\text{shift amount} = |(p - i) \bmod B|$$

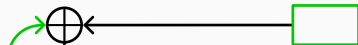
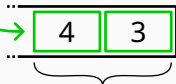
operand1

1332	862	302	1402	239	819	265	1053
------	-----	-----	------	-----	-----	-----	------

operand2

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

barrel shifter



accumulator

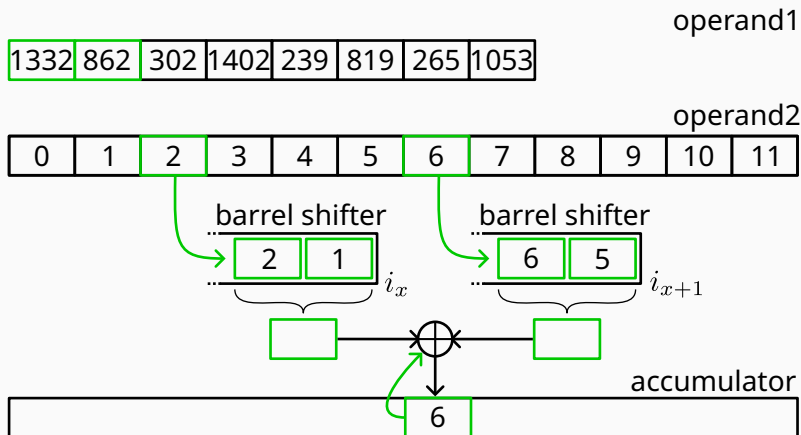
2

Polynomial multiplier: $R \times R_w$

Multiple indexes processed

$$\text{start block} = \lfloor (p - i) / B \rfloor$$

$$\text{shift amount} = \lfloor (p - i) \bmod B \rfloor$$

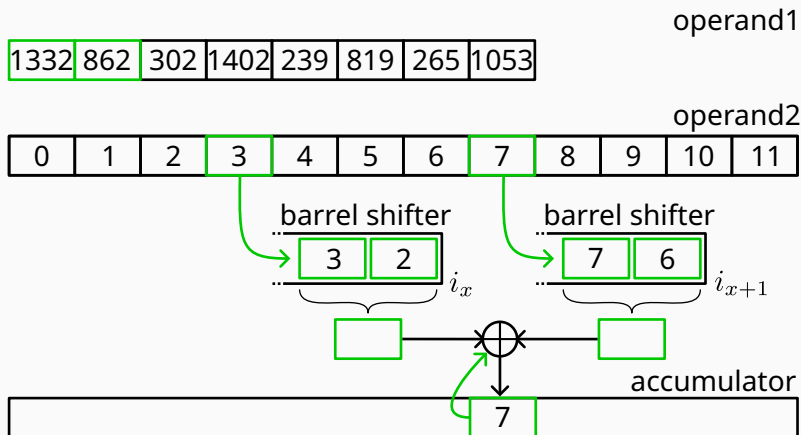


Polynomial multiplier: $R \times R_w$

Multiple indexes processed

$$\text{start block} = \lfloor (p - i) / B \rfloor$$

$$\text{shift amount} = \lfloor (p - i) \bmod B \rfloor$$



Sample random polynomials uniformly

Dense random polynomials in R

The elements of the binary vector $h \in R$ are generated by the SHAKE-256 algorithm (a SHA-3 eXtensible Output Function) expanding the small 320-bits public seed.

The output is trimmed to the correct bit size, padding with zero bits if the last block is underfilled.

Sample random polynomials uniformly

Sparse random polynomials in R_w

The HQC specification uses the constant-time algorithm from [16]:

- runs in constant-time
- uses of an exact amount of randomness ($32 \cdot w$ bits)
- requires a modulo operations between a 32-bit dividend and a generic 16-bit divisor

We used a straightforward *shift-and-subtract* pipelined algorithm, not requiring DSPs to perform the operation.

At synthesis time the number of pipeline stages can be selected to balance resources usage and timing closure.

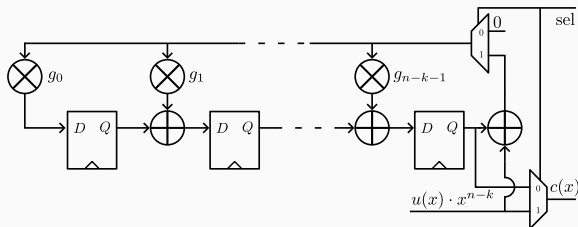
Public code: Reed Solomon Encoder

The code treats a block of data as a set of $\mathbb{F}_{2^8}$ elements (symbols).

In a systematic encoding procedure the sequence of symbols of the message polynomial $u(x)$ are the prefix of the codeword, and the error correcting symbols are the suffix:

$$c(x) = x^{n_e - k_e} u(x) - \left(x^{n_e - k_e} u(x) \bmod g(x) \right)$$

A simple way to produce such special encoding is through a Linear Feedback Shift Register [17]:



Consider a valid codeword $c(x)$ affected by an unknown error $e(x)$ which has up to t terms:

$$r(x) = c(x) + e(x)$$

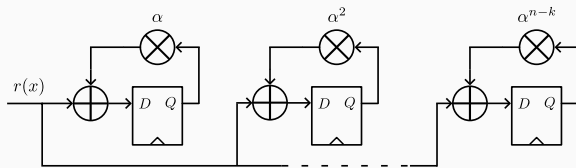
Decoding algorithm overview

The decoder computes:

- the polynomial associated to the syndrome of the received word $r(x)$
- both positions and values of the coefficients of $e(x)$
- the error-free codeword is derived as $c(x) = r(x) - e(x)$.

Public code: Reed Solomon Decoder

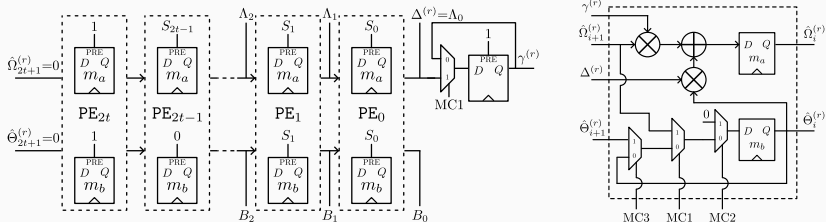
First, the received polynomial $r(x)$ is evaluated at each root α^i of the generator polynomial $g(x)$ using the Horner's method, determining the *syndrome polynomial* $S(x)$



Public code: Reed Solomon Decoder

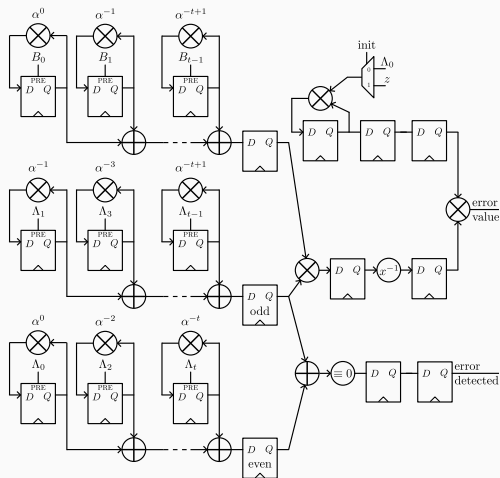
We employed the design of the Enhanced Parallel Inversionless Berlekamp-Massey Algorithm (ePIBMA) introduced in [18].

The *error locator polynomial* $\Lambda(x)$ and the *auxiliary polynomial* $B(x)$ are derived from the syndrome polynomial $S(x)$



Public code: Reed Solomon Decoder

Similarly, we used the Enhanced Chien Search and Error Evaluator design from [18] to compute the *error evaluator polynomial* $\Omega(x)$ from $\Lambda(x)$ and $B(x)$.



Public code: Reed Muller Encoder

To derive the 128-bit codewords corresponding to each 8-bit input message, we follow the traditional message vector multiplied by the generator matrix G_{RM} .

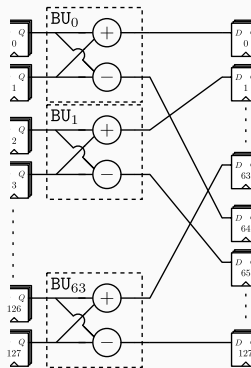
$$G_{RM} = \begin{bmatrix} 0xAAAAAAAA & 0xAAAAAAAA & 0xAAAAAAAA & 0xAAAAAAAA \\ 0xCCCCCCCC & 0xCCCCCCCC & 0xCCCCCCCC & 0xCCCCCCCC \\ 0xF0F0F0F0 & 0xF0F0F0F0 & 0xF0F0F0F0 & 0xF0F0F0F0 \\ 0xFF00FF00 & 0xFF00FF00 & 0xFF00FF00 & 0xFF00FF00 \\ 0xFFFF0000 & 0xFFFF0000 & 0xFFFF0000 & 0xFFFF0000 \\ 0x00000000 & 0xFFFFFFFF & 0x00000000 & 0xFFFFFFFF \\ 0x00000000 & 0x00000000 & 0xFFFFFFFF & 0xFFFFFFFF \\ 0xFFFFFFFF & 0xFFFFFFFF & 0xFFFFFFFF & 0xFFFFFFFF \end{bmatrix}$$

Working with 32-bits words, the presence of repeated words in G_{RM} yields some identical intermediate values during the multiplication.

Consequently, the size of multiplexers and the number of XOR gates were decreased substantially.

Public code: Reed Muller Decoder

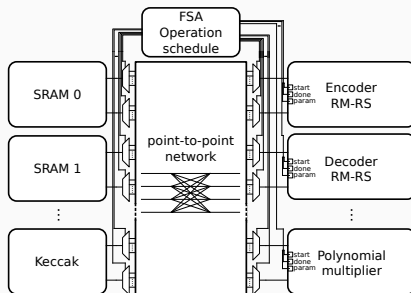
The operation is carried out by a Maximum Likelihood (ML) decoder computing a fast Hadamard transform [19]



We find the maximum absolute value with a pipelined comparator tree computing pairwise maxima, acting on a tunable-sized input vector.

Operation schedule

Top-Level Design configuration

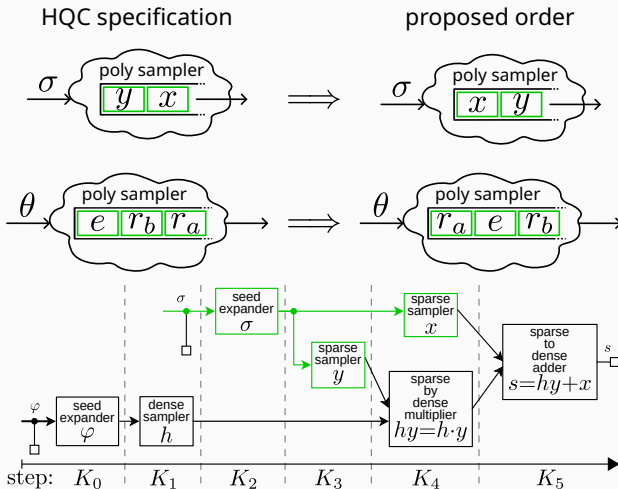


Top-Level Design (TLD) configuration implementing a KEM primitive.

We employed five True Dual-Port memories, which are connected in every moment to a specific compute unit (e.g., polynomial multiplier) by global Finite State Automata (FSA) following a fixed schedule of operations.

Operation schedule

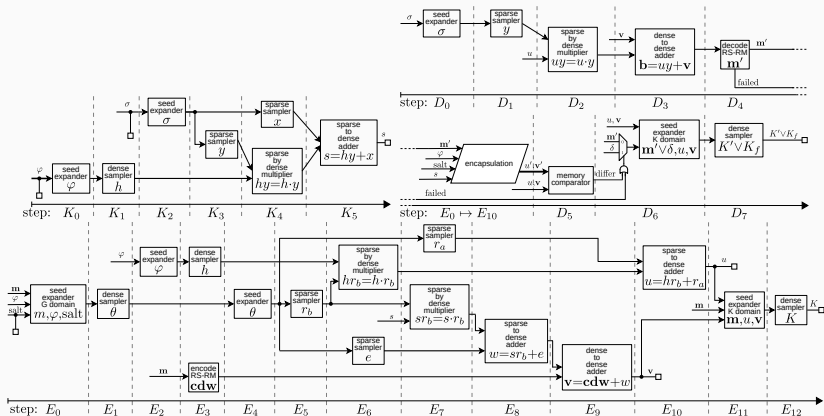
Sampling order optimization



Performance gains from 13% to 32% over the entire cryptographic primitive **without any cost or security implications**

Operation schedule

HQC.KEM schedules



Designed in SystemVerilog, tested with CocoTB following the Universal Verification Methodology (UVM).

Synthesized on an AMD Artix-7 xc7a200tfbg484-3 FPGA, and validated it on a Digilent's Arty A7-100T employing the (modified) official Known Answer Tests (KAT) via a UART module.

The source code is available on Zenodo.

Experimental results

Top-level: Key Generation

HQC keygen top-modules w/o SHAKE256 (5520 LUTs, 2810 FFs).

Parameter set	Design	Area eSlice	Frequency MHz	Latency μs	Area-Time product
hqc128	[20]	1879	179	88	165
	[21] (HLS, perf.)	2849	150	270	768
	This work	4267	208	30	127
hqc192	[20]	1866	189	222	415
	This work	4348	207	72	314
hqc256	[20]	1866	188	437	817
	This work	4272	201	138	591

Experimental results

Top-level: Encapsulation

HQC encapsulation top-modules w/o SHAKE256 (5520 LUTs, 2810 FFs).

Parameter set	Design	Area eSlice	Frequency MHz	Latency μs	Area-Time product
hqc128	[20] (balanced)	2701	179	186	504
	[20] (high speed)	3377	179	125	423
	[21] (HLS, perf.)	4575	152	586	2682
	This work	4326	168	79	343
hqc192	[20] (balanced)	2990	182	496	1484
	[20] (high speed)	3785	196	292	1106
	This work	4468	175	180	803
hqc256	[20] (balanced)	3123	182	973	3039
	[20] (high speed)	3901	196	553	2160
	This work	4412	187	313	1382

Experimental results

Top-level: Decapsulation

HQC decapsulation top-modules w/o SHAKE256 (5520 LUTs, 2810 FFs).

Parameter set	Design	Area eSlice	Frequency MHz	Latency μs	Area-Time product
hqc128	[20] (balanced)	4806	192	251	1206
	[20] (high speed)	5556	179	207	1154
	[21] (HLS, perf.)	6130	152	1270	7787
	This work	5956	167	119	709
hqc192	[20] (balanced)	5309	186	676	3590
	[20] (high speed)	6051	186	498	3018
	This work	7068	161	287	2026
hqc256	[20] (balanced)	5549	186	1335	7408
	[20] (high speed)	6289	186	966	6076
	This work	8098	151	570	4614

Experimental results

Top-level: unified design

Comparison of the unified designs compatible with all KEM primitives for parameter set guaranteeing a security similar to AES-128¹.

scheme	Design		Area eSlice	Freq. MHz	KeyGeneration		Encapsulation		Decapsulation	
	ref.	variant			μs	AT	μs	AT	μs	AT
Kyber	[22]	–	4147	220	10	40	15	62	20	85
Kyber	[23]	–	2758	161	24	65	32	87	42	115
HQC	This work	–	12471	143	39	488	82	1027	128	1597
HQC	[20]	balanced	10406	164	96	1000	204	2122	294	3059
HQC	[20]	high-speed	11167	178	89	989	126	1407	209	2333
HQC	[24]	–	20564	178	112	2311	225	4621	393	8087
BIKE	[25]	lightweight	5930	121	3826	22691	446	2646	6950	41216
BIKE	[25]	trade-off	9717	100	1870	18171	280	2721	4210	40909
BIKE	[25]	high-speed	15344	113	1681	25800	133	2037	1168	17924
C. McEliece	[26]	lightweight	36007	112	1161	41794	1518	54653	79286	2854841
C. McEliece	[26]	high-speed	48173	113	265	12789	885	42631	8584	413520

¹Highlighted designs support also security margins of AES-192 and AES-256.

Experimental results

ASIC synthesis

ASIC synthesis of top-level HQC.KEM designs using Yosys and *OpenROAD* with *FreePDK45* tech library and typical process corner 1.1V @ 25°C.

Design	Frequency (MHz)	Area mm ²
Key generation	502	0.235
Encapsulation	390	0.280
Decapsulation	457	0.469
Unified	419	0.496

Experimental results

Comparison with a SW execution

Comparing the execution runtime of the three KEM primitives with a software execution of the reference C code on a Rockchip RK3288 ARM Cortex-A17 CPU at 1.8GHz, our hardware accelerator is from $15.6\times$ to $19.8\times$ faster.

This target was chosen because it is produced with a 28nm process node technology similar to the one used for the AMD Artix-7 XC7A35T, and it has a similar bulk price of 20 US \$.

Producing an ASIC version of the design on a modern process node, the performance advantage will inevitably grow due to the higher working frequencies.

CROSS: Codes and Restricted Objects Signature Scheme

The Codes and Restricted Objects Signature Scheme (CROSS) scheme is a digital signature algorithm proposed in the additional NIST call for digital signatures relying on the NP-complete Restricted Syndrome Decoding Problem (R-SDP).

It is built applying the Fiat-Shamir construction to transform the CROSS-ID Zero-Knowledge (ZK) identification protocol into a non-interactive one using a one-way function and achieving the EUF-CMA security.

Introduction to CROSS

The Restricted Syndrome Decoding Problem – search variant

- $H \in \mathbb{F}_p^{(n-k) \times n}$ of a p -ary $[n, k, d]$ public random linear code
- $e \in E^n \subset \mathbb{F}_p^n$ the secret error vector from a subgroup of $\mathbb{F}_p^n$
- $s = eH^\top \in \mathbb{F}_p^{n-k}$ the syndrome associated to the error e

The subgroup E is generated by the public element g of order z :

$$\langle g \rangle = \{g^i \mid i \in \{1, \dots, z\}\} = E \subset \mathbb{F}_p^*$$

Given $pk = (H, s)$, find a vector $e \in E^n$ such that $s = eH^\top$.

The removal of the fixed-weight constraint in favor of the restriction of the ambient space of the error vector allowed to speed-up the computation and reduce the signature size.

Algebraic structure

- $E = \langle g \rangle = \{g^i \mid i \in \{1, \dots, z\}\} \subset \mathbb{F}_p^*$

Vector arithmetic modulo a prime $p \in \{127, 509\}$: $+$, $-$, $\odot$, $g^{(\cdot)}$

Algebraic structure

- $E = \langle g \rangle = \{g^i \mid i \in \{1, \dots, z\}\} \subset \mathbb{F}_p^*$

Vector arithmetic modulo a prime $p \in \{127, 509\}$: $+$, $-$, $\odot$, $g^{(\cdot)}$

$a \in E^n$ compactly represented by an element $\bar{a} \in \mathbb{F}_z^n$, $z \in \{7, 127\}$

$(E^n, \odot)$ isomorphic to $(\mathbb{F}_z^n, +)$: $a \odot b = g^{\bar{a} + \bar{b}}$, $a^{-1} = g^{-\bar{a}}$

Algebraic structure

- $E = \langle g \rangle = \{g^i \mid i \in \{1, \dots, z\}\} \subset \mathbb{F}_p^*$
- $G = \langle \{b_1, \dots, b_m\} \rangle = \{\odot_{i=1}^m b_i^{u_i} \mid b_i \in E^n \wedge u_i \in \mathbb{F}_z^* \wedge m < n\} \subset E^n$

Vector arithmetic modulo a prime $p \in \{127, 509\}$: $+$, $-$, $\odot$, $g^{(\cdot)}$

$a \in E^n$ compactly represented by an element $\bar{a} \in \mathbb{F}_z^n$, $z \in \{7, 127\}$

$(E^n, \odot)$ isomorphic to $(\mathbb{F}_z^n, +)$: $a \odot b = g^{\bar{a} + \bar{b}}$, $a^{-1} = g^{-\bar{a}}$

$\bar{M} = [\bar{b}_1, \dots, \bar{b}_m]^T$ with exponents of the bases, $a = g^{\bar{a}_G \bar{M}}$, $\bar{a}_G \in \mathbb{F}_z^m$

Algebraic structure

- $E = \langle g \rangle = \{g^i \mid i \in \{1, \dots, z\}\} \subset \mathbb{F}_p^*$
- $G = \langle \{b_1, \dots, b_m\} \rangle = \{\odot_{i=1}^m b_i^{u_i} \mid b_i \in E^n \wedge u_i \in \mathbb{F}_z^* \wedge m < n\} \subset E^n$

Vector arithmetic modulo a prime $p \in \{127, 509\}$: $+$, $-$, $\odot$, $g^{(\cdot)}$

$a \in E^n$ compactly represented by an element $\bar{a} \in \mathbb{F}_z^n$, $z \in \{7, 127\}$

$(E^n, \odot)$ isomorphic to $(\mathbb{F}_z^n, +)$: $a \odot b = g^{\bar{a} + \bar{b}}$, $a^{-1} = g^{-\bar{a}}$

$\bar{M} = [\bar{b}_1, \dots, \bar{b}_m]^\top$ with exponents of the bases, $a = g^{\bar{a}_G \bar{M}}$, $\bar{a}_G \in \mathbb{F}_z^m$

The linear transitive maps $v : E^n \mapsto E^n$ and $v_G : G \mapsto G$ are simply $v(a) = v \odot a = g^{\bar{v} + \bar{a}}$

The underlying hard problem is tweaked by selecting:

- the error vector ambient space E^n or G , for R-SDP and R-SDP(G) respectively
- a different parametrization of the random $[n, k, d]$ random linear code
- the number of CROSS-ID ZK protocol repetitions t

Background

CROSS-ID ZK protocol

CROSS-ID ZK protocol

Require: $sk = e \in G \subseteq \mathbb{E}^n$

$$pk = \left(H \in \mathbb{F}_p^{(n-k) \times n}, s = eH^T \in \mathbb{F}_p^{n-k} \right)$$

PROVER $\mathcal{P}$

VERIFIER $\mathcal{V}$

$$seed \xleftarrow{\$} \{0,1\}^\lambda$$

Commitment

$$e', u' \leftarrow \text{CSPRNG}(seed, G \times \mathbb{F}_p^n)$$

$$v \leftarrow e \odot (e')^{-1}$$

$$u \leftarrow v \odot u'$$

$$s' \leftarrow uH^T$$

$$cmt_0 \leftarrow \text{Hash}(s' \| v)$$

$$cmt_1 \leftarrow \text{Hash}(u' \| e')$$

$$\begin{array}{c} cmt_0, cmt_1 \\ \xrightarrow{\text{commitment}} \end{array}$$

First challenge

$$\begin{array}{c} chall_1 \\ \xleftarrow{1^{st} \text{ challenge}} \end{array}$$

$$chall_1 \xleftarrow{\$} \mathbb{F}_p^*$$

$$y \leftarrow u' + chall_1 e'$$

$$dig_y \leftarrow \text{Hash}(y)$$

$$\begin{array}{c} dig_y \\ \xrightarrow{1^{st} \text{ response}} \end{array}$$

Second challenge

$$\begin{array}{c} chall_2 \\ \xleftarrow{2^{nd} \text{ challenge}} \end{array}$$

$$chall_2 \xleftarrow{\$} \{0,1\}$$

$$\text{if } chall_2 = 0 \text{ then } resp \leftarrow y \| v$$

$$\text{else } resp \leftarrow seed$$

$$\begin{array}{c} resp \\ \xrightarrow{2^{nd} \text{ response}} \end{array}$$

Verification

if $chall_2 = 0$ then

$$y' \leftarrow v \odot y$$

$$s' \leftarrow y'H^T - chall_1 s$$

if $\text{Hash}(y) \neq dig_y \vee \text{Hash}(s' \| v) \neq cmt_0 \vee v \notin G$ then fail

else

$$(e', u') \leftarrow \text{CSPRNG}(seed, G \times \mathbb{F}_p^n)$$

$$y \leftarrow u' + chall_1 e'$$

if $\text{Hash}(y) \neq dig_y \vee \text{Hash}(u' \| e') \neq cmt_1$ then fail

The t rounds are performed in parallel, and commitments are transmitted only if the Verifier cannot recompute them.

When the second challenge is unbalanced (w out of t binary challenges are 1), the Prover will send more frequently the round seed, which is far smaller than $y||v$.

Warning

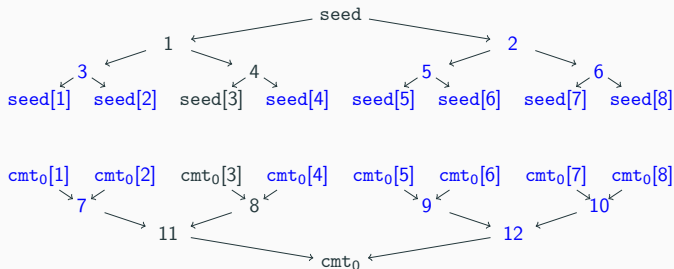
This requires to increase the number of protocol repetitions t to maintain the same security, hence trades a higher execution runtime for a smaller signature

Background

Optimization corners

Round seeds can be generated via the expansion of a master seed in a binary tree shape.

Analogously, `cmt0` of each round can be pre-combined during the signature generation using a Merkle tree.



CROSS seed and commitment trees

Hardware design

Vector addition/subtraction, and point-wise multiplication

The element-wise modular operations are carried out in parallel: for $p, z \in \{7, 127, 509\}$, a 64-bits word encodes 21, 9, and 7 elements.

The mod7 and mod127 reduction uses the efficient Mersenne prime reduction, and employs only a few adders.

By contrast, for mod509 the Barrett reduction employs two integer multiplications (the first one having a large output domain).

The operation is repeated until all the n or $m < n$ vector elements are processed.

Leveraging the small values of p , z and the fixed public generator g , the scalar operation $g^a \bmod p$ is performed via a look-up table.

z table entries of $\log_2 p$ bits $\rightarrow$ only 7 or 18 LUT FPGA units!

9, and 7 parallel operations can be performed each clock cycle, but an input FIFO is necessary due to the different read/write rates.

Hardware design

Vector-matrix multiplications

$$H^T = [V^T \mid I_{n-k}] = \begin{bmatrix} V_{0,0}^T & V_{0,1}^T & \cdots & V_{0,n-k-1}^T \\ V_{1,0}^T & V_{1,1}^T & \cdots & V_{1,n-k-1}^T \\ \vdots & \vdots & \ddots & \vdots \\ V_{k-1,0}^T & V_{k-1,1}^T & \cdots & V_{k-1,n-k-1}^T \\ 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix}$$

$$\bar{M} = [\bar{W}, \bar{I}_m] = \begin{bmatrix} \bar{W}_{0,0} & \bar{W}_{0,1} & \cdots & \bar{W}_{0,n-m-1} & 1 & 0 & \cdots & 0 \\ \bar{W}_{1,0} & \bar{W}_{1,1} & \cdots & \bar{W}_{1,n-m-1} & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \bar{W}_{m-1,0} & \bar{W}_{m-1,1} & \cdots & \bar{W}_{m-1,n-m-1} & 0 & 0 & \cdots & 1 \end{bmatrix}$$

Both matrices are serialized row-wise.

Hardware design

Vector-matrix multiplications

Leveraging their systematic form to avoid part of the computation.

$$\bar{e} = \bar{e}_G \bar{M} = \bar{e}_G [\bar{W}, \bar{I}_m] = [\bar{e}_G \bar{W}, \bar{e}_G]$$

Takes only $O(m(n - m)) < O(mn)$ multiplications in $\mathbb{F}_z$

$$s = eH^\top = e[V \mid I_{n-k}] = [e_k, e_{k+1}, \dots, e_n] + [e_0, e_1, \dots, e_{k-1}]V^\top$$

Takes only $O(k(n - k)) < O(n(n - k))$ multiplications in $\mathbb{F}_p$

Vector operator and result are transferred using 64-bits words.

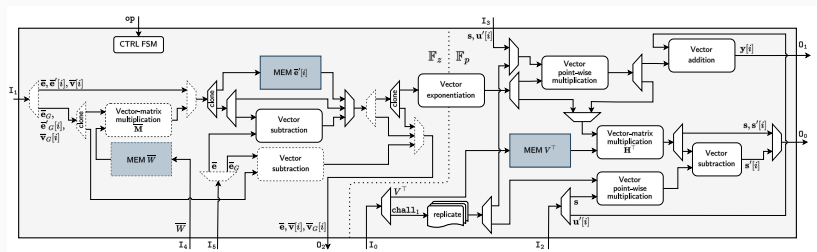
Matrices $V^\top$ and $\bar{W}$ are accessed using 64-bits, 192-bits, or enough bits in order to perform an entire row-by-coefficient computation.

Different levels of computational parallelism with this design choice.

Hardware design

Arithmetic unit

Following the order of operations in the three DSA operations (KeyGeneration, Sign, Verify), we chained the arithmetic units to limit the memory transfers and maximize the performance.



We used two local memories to store the serialized matrices employed during the t CROSS-ID rounds, and cache the (expanded) round errors $\bar{e}'$.

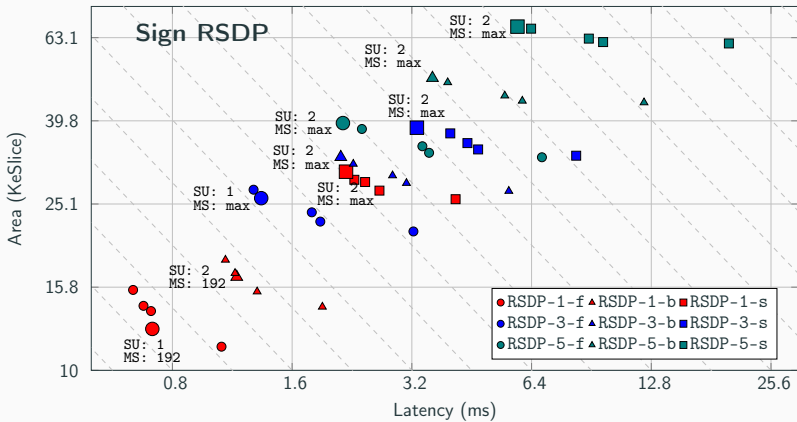
Designed in SystemVerilog, tested with CocoTB employing the reference software via ctypes function bindings.

Synthesized on various FPGAs of the AMD Artix-7 family, and validated it on a Digilent's Nexys Video employing the official Known Answer Tests (KAT) via a UART module.

We conducted a Design Space Exploration to determine Area/Latency trade points by varying:

- the parallelism of the matrix-vector multiplication
- the number of SHAKE-256 rounds per clock cycle

Artix-7 FPGA synthesis results¹

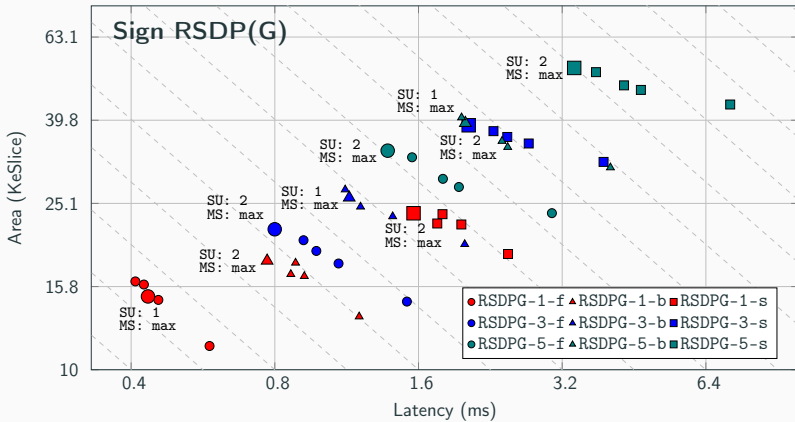


Design Space Exploration

¹Credits to Patrick Karl from the Technical University of Munich.

Experimental results

Artix-7 FPGA synthesis results¹

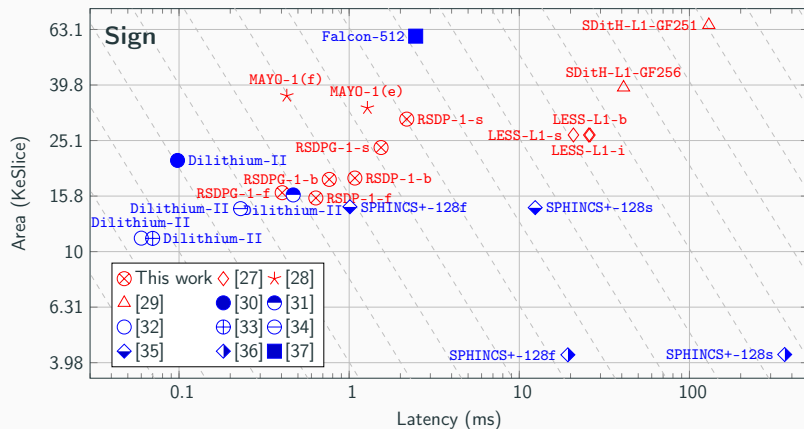


Design Space Exploration

¹Credits to Patrick Karl from the Technical University of Munich.

Experimental results

Artix-7 FPGA synthesis results¹



Comparison with other DSA – Security level AES-128

¹ Credits to Patrick Karl from the Technical University of Munich.

Experimental results

Comparison with a SW execution¹

Comparing the execution runtime of the three DSA primitives with a software execution of the reference C code on a Broadcom BCM2837B0 ARM Cortex-A53 CPU at 1.4GHz, our hardware accelerator produces a signature of a 59 bytes message from $2.3\times$ to $22.7\times$ faster.

This target was chosen due to being the only datapoint available right now in the SUPERCOP open cryptographic benchmarking tool for a low-end platform produced in a similar technology node and having a similar bulk price.

Producing an ASIC version of the design on a modern process node, the performance advantage will inevitably grow due to the higher working frequencies.

¹Credits to Marco Gianvecchio from Politecnico di Milano.

Concluding remarks

We presented a systematic approach for the analysis, design, and optimization of hardware accelerators for three PQC algorithms: the lattice-based KEM.NTRU, the code-based KEM.HQC, and the code-based DSA.CROSS.

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Leveraging the data parallelisms offered by the sub-algorithms and the parallel schedule of operations in the KEM/DSA primitives, we set up design-space experiments to determine the solutions with interesting latency and efficiency figures.

Concluding remarks

We presented a systematic approach for the analysis, design, and optimization of hardware accelerators for three PQC algorithms: the lattice-based KEM.NTRU, the code-based KEM.HQC, and the code-based DSA.CROSS.

Leveraging the data parallelisms offered by the sub-algorithms and the parallel schedule of operations in the KEM/DSA primitives, we set up design-space experiments to determine the solutions with interesting latency and efficiency figures.

The produced hardware accelerators distinguished for their low primitive execution latency, higher efficiency, and high flexibility.



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Thanks for your attention!

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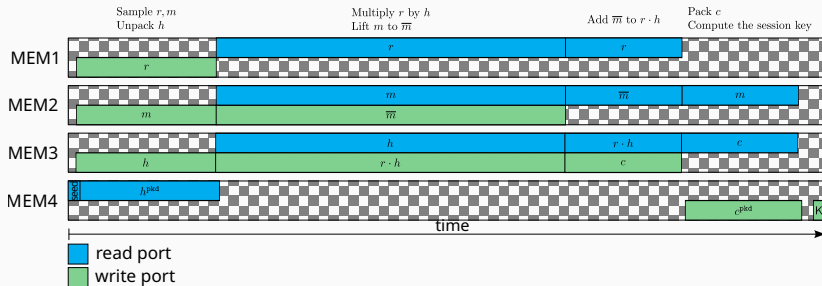
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Backup slides

Memory constraints

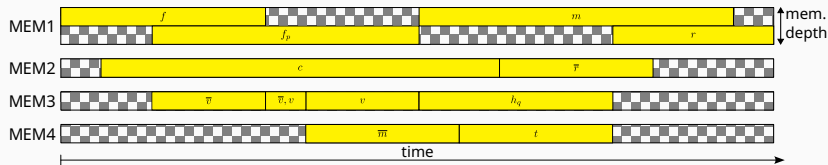
Memory access constraint (memory port binding)



Binding of operations to memory ports for the **NTRU-HRSS encapsulation** algorithm

Memory constraints

Memory size constraint (variable liveness)



Variable liveness analysis for the **NTRU-HPS decapsulation** algorithm

CROSS – Experimental results

Artix-7 FPGA synthesis results²

Design	Parameter set	Area eSlice	Freq. MHz	KeyGen.		Sign		Verify	
				μ S	AT	μ S	AT	μ S	AT
This work	CROSS-RSDP-1-f	13087	119	35	467	764	10006	584	7653
	CROSS-RSDP-1-b	15889	113	37	596	1444	22951	1016	16157
	CROSS-RSDP-1-s	27462	115	36	1013	2858	78508	1960	53841
	CROSS-RSDP-3-f	22885	110	82	1886	1905	43609	1455	33310
	CROSS-RSDP-3-b	28283	108	84	2380	3230	91355	2067	58488
	CROSS-RSDP-3-s	34120	105	86	2949	4984	170081	3037	103653
	CROSS-RSDP-5-f	33591	105	153	5170	3762	126370	2843	95514
	CROSS-RSDP-5-b	44720	101	160	7157	6297	281646	3744	167460
This work	CROSS-RSDP-5-s	61796	101	160	9887	10153	627431	5564	343849
	CROSS-RSDPG-1-f	15452	100	10	163	601	9300	477	7376
	CROSS-RSDPG-1-b	17396	103	10	178	1216	21154	886	15421
	CROSS-RSDPG-1-s	23005	102	10	239	2433	55979	1762	40540
	CROSS-RSDPG-3-f	18377	96	22	413	1260	23162	1033	18998
	CROSS-RSDPG-3-b	23795	102	21	503	1604	38185	1201	28593
	CROSS-RSDPG-3-s	35344	99	21	770	3103	109699	2214	78267
	CROSS-RSDPG-5-f	27749	99	35	997	2223	61701	1860	51637
[30]	CROSS-RSDPG-5-b	34512	96	37	1278	2960	102183	2222	76717
	CROSS-RSDPG-5-s	47332	98	36	1715	5133	242993	3613	171042
	Dilithium-II			12.2	260	98.3	2096	14.4	307
[31]	Dilithium-III	21330	185	22.6	482	166.7	3555	25.4	541
	Dilithium-V			30.3	646	196.3	4187	33.2	708
[31]	Dilithium-II	16091	163	115	1850	178/470	2864/7562	121	1947
	Dilithium-III	18230	145	228	4156	310/850	5651/15495	221	4028
	Dilithium-V	23788	140	363	8635	503/1042	11965/24787	377	8968
[38]	Dilithium-V	21597	116	121	2613	2520	54424	21	453
[35]	SPHINCS+-128f-s	14571	250/500	–	–	1010	14716	16	233
	SPHINCS+-192f-s	15838	250/500	–	–	1170	18530	19	300
	SPHINCS+-256f-s	17657	250/500	–	–	2520	44495	21	370

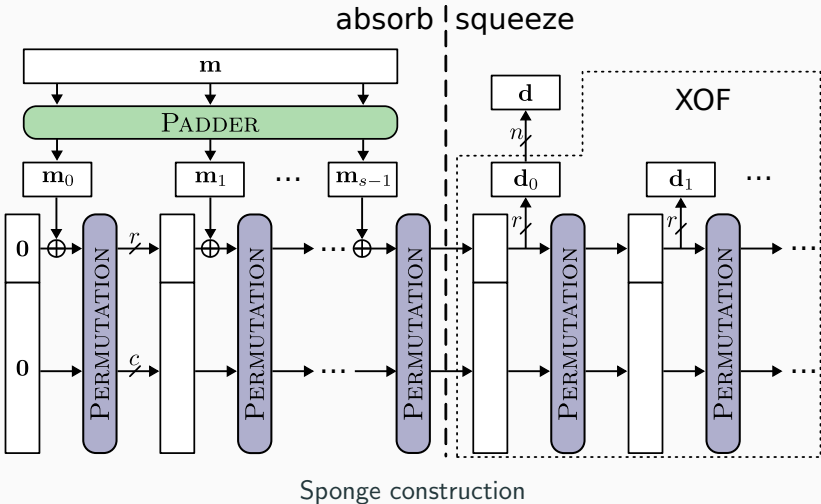
² Credits to Patrick Karl from the Technical University of Munich.

Assessment multiplier algorithms for HQC

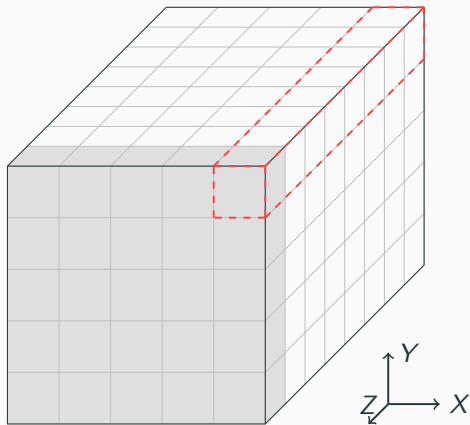
We simulated different approaches for the $\mathbb{F}_2[x]$ multiplications required in the code-based HQC cryptoscheme.

Block size	Mult. algorithm	Latency (kCC)		
		hqc-128	hqc-192	hqc-256
32	Comba	305.80	1256.64	3247.20
32	Karatsuba 5-terms + NTT	76.03	230.91	464.64
32	Karatsuba 5-terms + Comba	237.31	714.75	1432.32
32	Rotate and accumulate (d=1)	41.47	127.79	268.49
32	Rotate and accumulate (d=2)	20.73	63.89	134.24
32	Rotate and accumulate (d=4)	10.36	31.94	67.12
64	Comba	76.72	314.72	811.80
64	Karatsuba 5-terms + NTT	34.43	104.70	210.81
64	Karatsuba 5-terms + Comba	61.31	185.34	372.09
64	Rotate and accumulate (d=1)	20.77	63.95	134.24
64	Rotate and accumulate (d=2)	10.38	31.97	67.12
64	Rotate and accumulate (d=4)	5.19	15.98	33.56
128	Comba	19.32	78.96	203.40
128	Karatsuba 5-terms + NTT	15.42	46.97	94.65
128	Karatsuba 5-terms + Comba	16.32	49.66	100.03
128	Rotate and accumulate (d=1)	10.42	32.03	67.19
128	Rotate and accumulate (d=2)	5.21	16.01	33.60
128	Rotate and accumulate (d=4)	2.60	8.00	16.80

Keccak core



Keccak core



Keccak state representation

Keccak FPGA cores synthesized on an Artix-7

Ref.	Design Type	Variant	Area			Frequency MHz	SHA3-256			
			LUT	FF	eSlice		CC	μ s	AT prod.	Gb/s
[39]	mid-range*	$\times 1$	811	490	203	178	2681	15.06	3.06	0.07
[20]	mid-range	$\times 1$	1437	498	360	163	2408	14.77	5.32	0.07
[39]	mid-range*	$\times 2$	908	450	227	163	1353	8.30	1.88	0.13
[20]	mid-range	$\times 2$	1558	466	390	167	1206	7.22	2.82	0.15
[39]	mid-range*	$\times 4$	1069	361	268	158	680	4.30	1.15	0.25
[20]	mid-range	$\times 4$	1625	370	407	157	604	3.85	1.57	0.28
[39]	mid-range*	$\times 8$	1466	270	367	164	337	2.05	0.75	0.52
[20]	mid-range	$\times 8$	1958	280	490	158	302	1.91	0.94	0.56
[39]	mid-range*	$\times 16$	2401	226	601	165	168	1.02	0.61	1.04
[20]	mid-range	$\times 16$	2819	236	705	164	150	0.91	0.64	1.17
[39]	mid-range*	$\times 32$	4436	180	1109	161	85	0.53	0.59	2.00
[20]	mid-range	$\times 32$	4797	191	1200	166	74	0.45	0.53	2.36
This work	high-speed	$\times 1$	5589	2744	1398	237	29	0.12	0.17	8.85
This work	high-speed	$\times 2$	10571	2736	2643	125	17	0.14	0.36	7.59
This work	high-speed	$\times 3$	12700	2719	3175	74	13	0.18	0.56	5.90
This work	high-speed	$\times 4$	15472	2717	3868	53	11	0.21	0.80	5.06
This work	high-speed	$\times 6$	22725	2715	5682	28	9	0.32	1.83	3.32
This work	high-speed	$\times 8$	20262	2714	5066	26	8	0.31	1.56	3.43
This work	high-speed	$\times 12$	28782	2713	7196	14	7	0.50	3.60	2.12
This work	high-speed	$\times 24$	55403	2714	13851	6	6	1.00	13.85	1.06