University LSI Design Contest

Title	:	**Design and simulation of an 8x8 Batcher-Banyan switch using ALTERA EPLD**
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Area	:	4-c (Custom application specific circuits in FPGA / PLD)

Brief Description:

The Batcher-Banyan network is a special class of multistage interconnection network mostly used in multiprocessor interconnections and in ATM switches. The switches designed for these applications need to be fully scalable. The main challenge was to design a switching element for a Batcher-Banyan network, which has the same property. The switching element designed could be used to implement networks of any size by only varying the input control signal and changing the external interconnections.

The main features of this design are

- It is a fully scalable
- Minimum buffering at each stage
- A distributed control unit is used

The design was mapped to a FLEX 10K EPLD and simulated in the ALTERA Max+plus II environment and was found to operate at 155Mbps.

Design and Simulation of an 8x8 Batcher-Banyan switch using ALTERA EPLD

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Abstract - The Batcher-Banyan (BB) network is an important class of non-blocking multistage interconnection networks widely used in shared memory multiprocessor interconnection and as well as in ATM switches. In this project, we implemented switching elements for these Batcher-Banyan networks. These switches were designed to be fully scalable so that the same switching element could be used for building large networks by only varying the input control signal and external interconnections. The control unit is fused with the switching element so that the main bottleneck due to complex interconnection of control signal is eliminated, which also ensures scalability. An 8x8 BB switch was designed, simulated and implemented using ALTERA Tools. The simulation results show that the switch can perform at line rates of 155Mbps which makes them suitable for ATM networks.

1. Introduction

The Batcher Banyan (BB) network is self-routing and configures itself in a distributed fashion based on the information carried in individual packet streams. The lowest element in the hierarchy of this network is the Switching Element (SE). When these SE's are suitably connected (Fig 2), they form an internally non-blocking, self-routing path for distinct sets of input address and are capable of routing the packets in parallel. Architecturally the BB network is fully scalable, so the main challenge in this project is to design the SE to be scalable with less buffering. It should be possible to build large networks of 1024 inputs without any change in the SE internally. Schemes suggested in [1] have been employed in the design of 8x8 BB switch along with the concept of distributed control unit. The control signals flow along with the data throughout the switch and therefore the data appears to be stationary with respect to the control signal.

1.1 Preliminaries

The Basic SE structure as shown in Fig. 1a can take either of the two states, pass (i_0 to o_0 and i_1 to o_1) or cross (i_0 to o_1 and i_1 to o_0). The algorithm executed by a given SE depends upon the state determination logic of the SE.

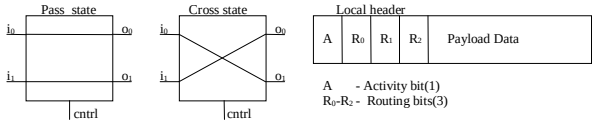

Fig 1a SE states. Fig 1b Input Packet format

The Batcher element sorts the packets according to the output address and the Banyan element delivers the packet to the required output address. The input packet format is shown in Fig. 1b. The activity bit is used to indicate the presence of valid data in the payload. The address or routing field contains the address of the output port to which the packet needs to be delivered. The payload might be an ATM cell or data to shared memory in multiprocessor architectures. The architecture of an 8x8 network built using this Batcher and Banyan SE element is shown in Fig 2.

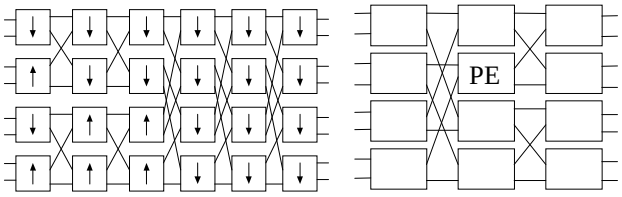

Fig. 2: 8x8 Batcher and Banyan Network

2. Batcher Switching Element

The Batcher SE performs a bit serial comparison of the input such that the packet with the largest binary address always exits at port o_0 for up-sort Batcher SE (denoted by up-pointing arrow) and at port o_1 for down-sort SE (denoted by down-pointing arrow). The block diagram of a Batcher SE is shown in Fig. 3. There are two states for the SE, the pass and the cross-state, as shown in Fig 1a. The circuit for a Batcher state determination logic (SDL) is shown in Fig. 4.

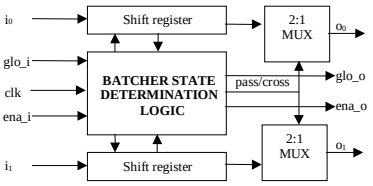

Fig. 3 Batcher switching element

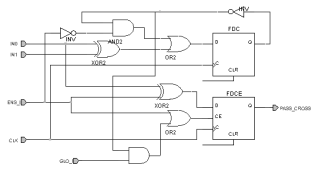

Fig. 4 Batcher SDL

2.1 Algorithm for implementation of the Batcher SDL

Step 1: when only one i/p is valid, it goes to the o/p o_0 for down-sort SE and to output o_1 in case of up-sort SE.

Step 2: when both the inputs have a valid data, then

- If they have the same bits just continue in pass/cross state as long as the i/p does not differ.
- If $i_1 > i_0$, i.e. if i_1 has '1' and i_0 has '0' then enforce the SDL to cross state in case of up-sort SE or to pass state in case of down-sort SE. This state is maintained for the entire packet length irrespective of the subsequent bits.
- When $i_0 > i_1$, then SDL goes to pass state for up-sort SE and to cross state for down-sort SE. Overall the packets are sorted based on the address bit scanned serially.

The signal *ena_i* indicates the presence of the activity bits in the incoming packet. The *glo_i* signal is high only for the packet header period and is used to terminate the entire bit

comparison circuitry after the routing and activity bits are scanned.

2.2 Features

Architecture implemented for the above algorithm has the following features:

- Bit serial comparison is performed with just a two-bit buffer until a difference is detected. Thus we reduce the buffer needed in each SE, and hence the propagation delays.
- No separate or common control block has been designed. All the functions for providing appropriate delay to *ena_i* and *glo_i* signals are in-built in single SE. This would prevent the need for complicated interconnection and helps in modular design. For designing any network, the input control signal *glo_i* only need to indicate the length of the header and nothing more. Since SE is not redesigned internally for network of different size it is fully scalable.

3. Banyan Switching Element

3.1 Introduction

The Banyan SE is a 2x2 switching element, which routes an incoming packet according to a control bit. If the control bit is 0, the cell is routed to the upper output port (address 0) otherwise the cell is routed to the lower output (address 1). The routing bits at a particular position determine the state of Banyan SE at a particular stage. The first stage of Banyan network routes according to the first routing bit, the second routes according to the second bit and so on. If straight-forward design of Banyan SE is carried then the 8x8 network requires a three-bit buffer and 1024 input network would require a 10 bit-buffer. Such type of SE is non-scalable. So in this design, after the state determination is made the SE moves the route bit of the next SE (fig. 1b) directly after the activity bit to make every banyan element identical and to minimize the buffering requirement [1].

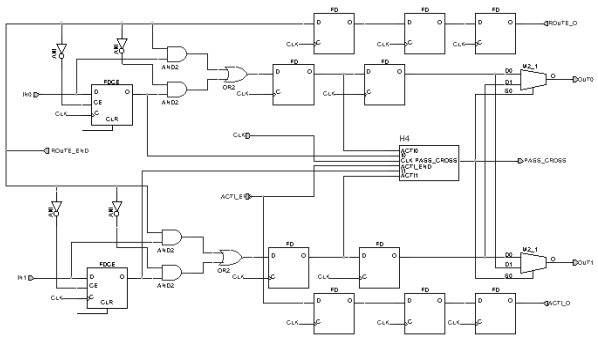

Fig. 5 Architecture of Banyan SE

3.2 Algorithm

1. Buffer the activity bit and the first routing bit
2. If only one of the input is active, route according to the routing bit at that input, e.g. if it is '1', route the packet to output o_1 and so on.
3. If the activity bits are same and routing bits differ then route according to one route bit.
4. If both the activity bits and route bits are same, then route randomly depending upon the previous state.
5. Disable the state determination and maintain the same pass/cross state for the entire cell period.
6. After the state determination is made, rotate the routing bits such that route bit of the next stage comes directly after the activity bit. The architecture of Banyan SE is shown in Fig. 5 and the simulation result in Fig. 6. Once the state of the SE is determined, we can observe that the routing bits are rotated at the input in0 and in1..

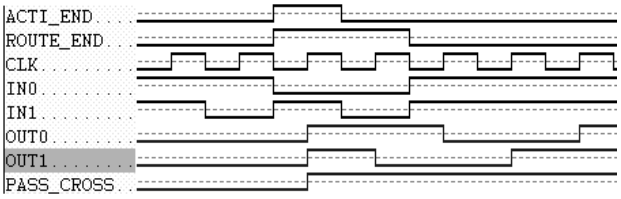

Fig. 6 Simulation output of Banyan SE

4. Results

An 8x8 BB chip (Fig. 2) was implemented using the Batcher and Banyan SE. The final chip block diagram is shown in Fig. 7 and the simulation result of the entire 8x8 switch is shown in Fig. 8. The final chip contains a block called the control transfer block, which translates the control *glo_ena* to *route_end* and *acti_end*, which controls the Banyan stage. The simulation results in Fig. 8 shows that when we apply the input data in a random order than the BB chip delivers the data to the required address. The final BB chip specification is shown in Table I

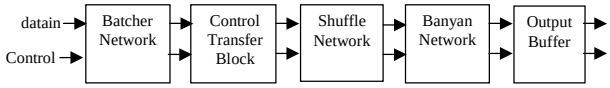

Fig. 7 Complete block diagram of the BB chip

TABLE I: Batcher-Banyan chip Specification

Device family used	FLEX 10K
Clock input interface	3.0 (min supply)
No. of input / output	8/8
Supply Voltage	3.3 V
Max. chip speed	160MHz
Maximum capacity	1.28Gbps
Logic Cells	429
Flip flops	390
Setup/hold time	4.4ns/0.0ns

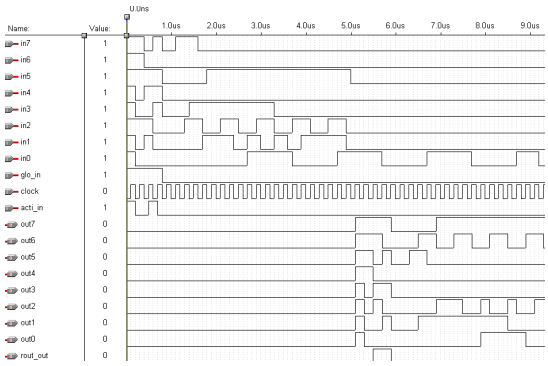

Fig. 8 Simulation result of the 8x8 Batcher-Banyan chip

Reference

[1]. William Marcus, "A CMOS Batcher-Banyan Chip Set for B-ISDN Packet Switching", Feb. 1990, *IEEE Transactions on Solid State Circuits.*